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ACOP

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CHANGE RECORD

ISSUE	*DATE*	*CHANGE AUTHORITY*	*REASON FOR CHANGE AND AFFECTED SECTIONS*
1	January 2005	-	First Issue
2	October 2005	Flight Safety Review 0/I and PDR outcomes	CDR Data Package. Document updated according to design changes after PDR and PDR comments and RIDs. General revision of the document, all pages affected

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1. SCOPE AND INTRODUCTION

This document defines and details the AMS-02 Crew Operation Post (ACOP) avionics design.

This report, issued for the program CDR, gives a general functional description, specification of ACOP and design information regarding the avionics design. Information on the overall ACOP design can be found in the ACOP Design Report.

2. DOCUMENTS

2.1 APPLICABLE DOCUMENTS

AD	Doc. Number	Issue / Date	Rev.	Title / Applicability
1	SSP 52000-IDD-ERP	D / 6.08.03		EXpedite the PRocessing of Experiments to Space Station (EXPRESS) Rack Payloads Interface Definition Document
2	NSTS/ISS 13830	C / 01.12.1996		Implementation Procedures for Payloads System Safety Requirements – For Payloads Using the STS & ISS.
3	JSC 26493	17.02.1995		Guidelines for the preparation of payload flight safety data packages and hazard reports.
4	SSP 50004	April 1994		Ground Support Equipment Design requirements
5	SSP-52000-PDS	March 1999	B	Payload Data Set Blank Book
6	SSP 57066	October 28, 2003		Standard Payload Integration Agreement for EXPRESS/WORF Rack Payloads
7	GD-PL-CGS-001	3 / 17.03.99		Product Assurance & Rams Plan
8	SSP 52000 PAH ERP	November 1997		Payload Accommodation Handbook for EXPRESS Rack
9	SSP 50184	D / February 1996		Physical Media, Physical Signaling & link-level Protocol Specification for ensuring Interoperability of High Rate Data Link Stations on the International Space Program
10	SSP 52050	D / 08.06.01		S/W Interface Control Document for ISPR ***ONLY FOR HRDL, SECTION 3.4 ***
11	ECSS-E-40	A / April 1999	13	Software Engineering Standard
12	AMS02-CAT-ICD-R04	29.08.2003	04	AMS02 Command and Telemetry Interface Control document. Section AMS-ACOP Interfaces
13	SSP 52000-PVP-ERP	Sept. 18, 2002	D	Generic Payload Verification Plan EXpedite the PRocessing of Experiments to Space Station (EXPRESS) Rack Payloads
14	NSTS 1700.7B	Rev. B Change Packet 8 / 22.08.00		Safety Policy and Requirements for Payloads using the STS
15	NSTS 1700.7B Addendum	Rev. B Change Packet 1 / 01.09.00		Safety Policy and Requirements for Payloads using the International Space Station
16	SSP 52005	Dec. 10, 1998		Payload Flight equipment requirements and guidelines for safety critical structures
17	NSTS 18798B	Change Packet 7 10.00		Interpretation of NSTS Payload Safety Requirements
18	MSFC-HDBK-527	15.11.86	E	Materials selection list for space hardware systems Materials selection list data
19	GD-PL-CGS-002	1 / 12.02.99		CADM Plan
20	GD-PL-CGS-004	2 / 07.04.03		SW Product Assurance Plan
21	GD-PL-CGS-005	2 / 09.05.03		SW CADM Plan

Table 2-1 Applicable Documents

2.2 REFERENCE DOCUMENTS

RD	Doc. Number	Issue / Date	Rev.	Title
1	GPQ-MAN-02	1		Commercial, Aviation and Military (CAM) Equipment Evaluation Guidelines for ISS Payloads Use
2	BSSC (96)2	1 / May 96		Guide to applying the ESA software engineering standards to small software projects
3	GPQ-MAN-01	2 / December 98		Documentation Standard for ESA Microgravity Projects
4	MS-ESA-RQ-108	1 / 28 Sept. 2000		Documentation Requirements For Small And Medium Sized MSM Projects
5	PSS-05			Software Engineering Standards
6	GPQ-010	1 / May 95	A	Product Assurance Requirements for ESA Microgravity Payload. Including CN 01.
7	GPQ-010-PSA-101	1		Safety and Material Requirements for ESA Microgravity Payloads
8	GPQ-010-PSA-102	1		Reliability and Maintainability for ESA Microgravity Facilities (ISSA). Including CN 01
9	SSP 52000-IDD-ERP	E / 09/09/03		EXpedite the PRocessing of Experiments to Space Station (EXPRESS) Rack Payloads Interface Definition Document
10	ACD-Requirements-Rev-BL	September 2005	Base Line	ACOP Common Design Requirements Document
11	ECSS-Q-60-11A	1 / 7 Sept. 2004		De-rating and End-of-life Parameter Drifts – EEE Components

Table 2-2 Reference Documents

3. DEFINITIONS AND ACRONYMS

A

AAA	Avionics Air Assembly
ABCL	As-Built Configuration data List
ACOP	AMS-02 Crew Operation Post
ACOP-SW	ACOP Flight Software
ADP	Acceptance Data Package
AMS-02	Alpha Magnetic Spectrometer 02
APS	Automatic Payload Switch
AR	Acceptance Review
ASI	Agenzia Spaziale Italiana *(Italian Space Agency)*
ATP	Authorization To Proceed

B

BC	Bus Coupler
BDC	Baseline Data Collection
BDCM	Baseline Data Collection Model

C

CAD	Computer Aided Design
CCB	Configuration Control Board
CCSDS	Consultative Committee on Space Data Standards (standard format for data transmission)
C&DH	Command & Data Handling
CDR	Critical Design Review
CGS	Carlo Gavazzi Space
CI	Configuration Item
CIDL	Configuration Item data List
CM	Configuration Management
COTS	Commercial Off The Shelf
cPCI	CompactPCI (Euro Card sized standard interface to the PCI)
CSCI	Computer Software Configuration Item
CSIST	Chung Shan Institute of Science and Technology

D

DCL	Declared Components List
DIL	Deliverable Items List
DIO	Digital Input / Output
DML	Declared Materials List
DMPL	Declared Mechanical Parts List
DPL	Declared Processes List
DRB	Delivery Review Board
DRD	Document Requirements Description

E

EEE	Electrical, Electronic & Electromechanical
EGSE	Electrical Ground Support Equipment
EM	Engineering Model
ER	EXPRESS Rack
ERL	EXPRESS Rack Laptop
ERLC	EXPRESS Rack Laptop Computer
ERLS	EXPRESS Rack Laptop Software
EMC	Electro-Magnetic Compatibility
ESA	European Space Agency
EXPRESS	EXpedite the PRocessing of Experiments to Space Station

F

FEM	Finite Element Model
FFMAR	Final Flight Model Acceptance Review
FLASH	Rewriteable persistent computer memory
FM	Flight Model
FMECA	Failure Modes, Effects & Criticalities Analysis
FPGA	Field Programmable Gate Array
FSM	Flight Spare Model

G

GIDEP	Government Industry Data Exchange Program
GSE	Ground Support Equipment

H

HCOR	HRDL Communications Outage Recorder
HD	Hard Drive
HDD	Hard Disk Drive
HRDL	High Rate Data Link
HRFM	High Rate Frame Multiplexer
HW	Hardware

I

ICD	Interface Control Document
I/F	Interface
IRD	Interface Requirements Document
ISPR	International Space-station Payload Rack
ISS	International Space Station

J

JSC	Johnson Space Center

K

KIP	Key Inspection Point
KSC	Kennedy Space Center
KU-Band	High rate space to ground radio link

L

LAN	Local Area Network
LCD	Liquid Crystal Display
LFM	Low Fidelity Model
LRDL	Low Rate Data Link

M

MDL	Mid-Deck Locker
MGSE	Mechanical Ground Support Equipment
MIP	Mandatory Inspection Point
MMI	Man Machine Interface
MPLM	Multi-Purpose Logistic Module
MRDL	Medium Rate Data Link

N

NA	Not Applicable
NASA	National Aeronautics and Space Administration
NCR	Non Conformance Report
NDI	Non Destructive Inspection
NRB	Non-conformance Review Board
NSTS	National Space Transportation System (Shuttle)

O

OLED	Organic Light-Emitting Diode
ORU	Orbital Replacement Unit

P

PA	Product Assurance
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect (personal computer bus)
PCS	Personal Computer System
PDR	Preliminary Design Review
PEHB	Payload Ethernet Hub Bridge
PEHG	Payload Ethernet Hub Gateway
PFMAR	Preliminary Flight Model Acceptance Review
PLMDM	Payload Multiplexer De-Multiplexer

PMC	PCI (Peripheral Component Interconnect) Mezzanine Card
PMP	Parts, Materials & Processes
PROM	Programmable Read Only Memory
PS	Power Supply

Q

QM	Qualification Model

R

RFA	Request For Approval
RFD	Request For Deviation
RFW	Request For Waiver
RIC	Rack Interface Controller
ROD	Review Of Design
ROM	Read Only Memory
RX	Reception

S

SATA	Serial Advanced Transfer Architecture (disk interface)
S-Band	Space to ground radio link
SBC	Single Board Computer
SC MDM	Station Control Multiplexer De-Multiplexer
ScS	Suitcase Simulator
SDD	Solid-state Disk Drive
SIM	Similarity Assessment
SIO	Serial Input Output
SOW	Statement Of Work
SPF	Single Point Failure
SRD	Software Requirements Document
STS	Space Transportation System (Shuttle)
SW	Software

T

TBC	To Be Confirmed
TBD	To Be Defined
TBDCM	Training & Baseline Data Collection Model
TBDCMAR	TBDCM Acceptance Review
TBP	To Be Provided
TCP/IP	Transmission Control Protocol / Internet Protocol
TFT	Thin Film Transistor
TM	Telemetry
TRB	Test Review Board
TRR	Test Readiness Review
TRM	Training Model
TX	Transmission

U

UIP	Utility Interface Panel
UMA	Universal Mating Assembly
USB	Universal Serial Bus

#

100bt	Ethernet 100Mbit Specification
1553	Reliable serial communications bus

4. DESCRIPTION OF ACOP

The ACOP System is a reliable special purpose computer intended to fly on the International Space Station (ISS) as a payload installed into an EXPRESS ISPR in the NASA US laboratory module. The main objective of ACOP is to provide an ISS Internal Facility capable of supporting AMS-02 experiment, performing the recording of Science data.

In particular, ACOP shall allow a more flexible and efficient use of ISS telemetry downlink, providing a backup of data generated by AMS-02 and preventing, in this way, possible losses of valuable data. In addition, ACOP provides a control and monitoring interface for the on-board crew to the external AMS payload. It also permits large software uploads into AMS.

ACOP is not designed to provide safety critical commands to AMS-02.

ACOP system shall be installed in the U.S. Laboratory Module, on the ISS, in one EXPRESS rack (see, for reference, Figure 4-1).

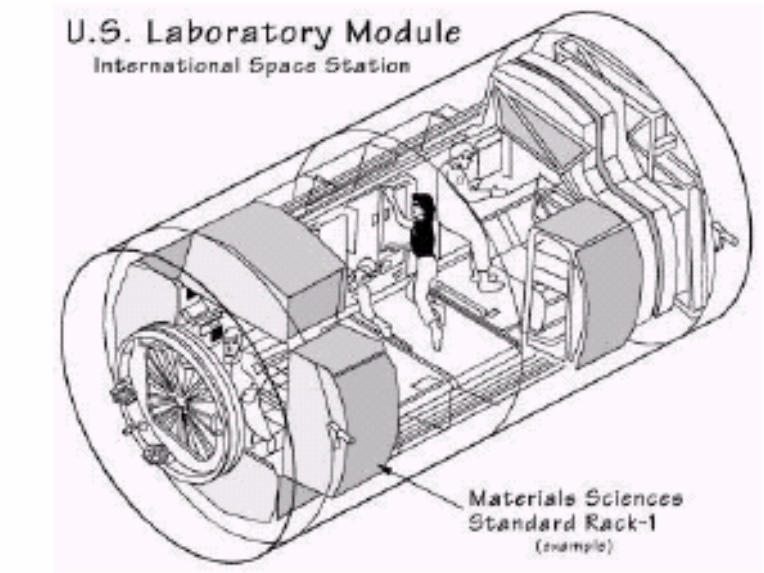

Figure 4-1 US-LAB

The standard configuration of an EXPRESS Rack is commonly known as 8/2. This means the rack can accommodate eight ISS Locker / Middeck Locker (MDL) units and two International Subrack Interface Standard (ISIS) units, as shown in Figure 4-2 and Figure 4-3. Figure 4-4 shows ACOP installed in such a rack (the location within the rack is just an example, the actual location will be determined by the ISS program).

On-board spare parts, including hard drives shall be accommodated in a standard soft bag.

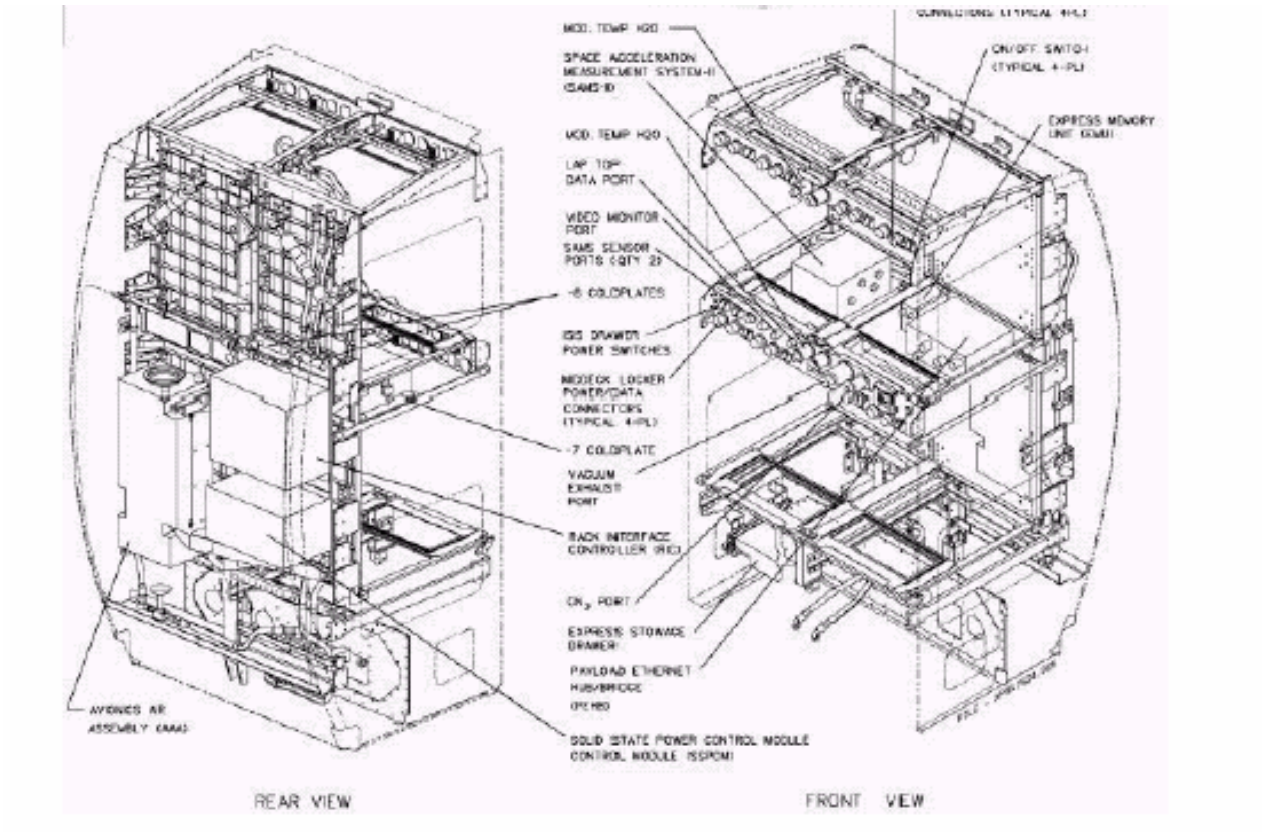

Figure 4-2 Example of an EXPRESS Rack (3D view)

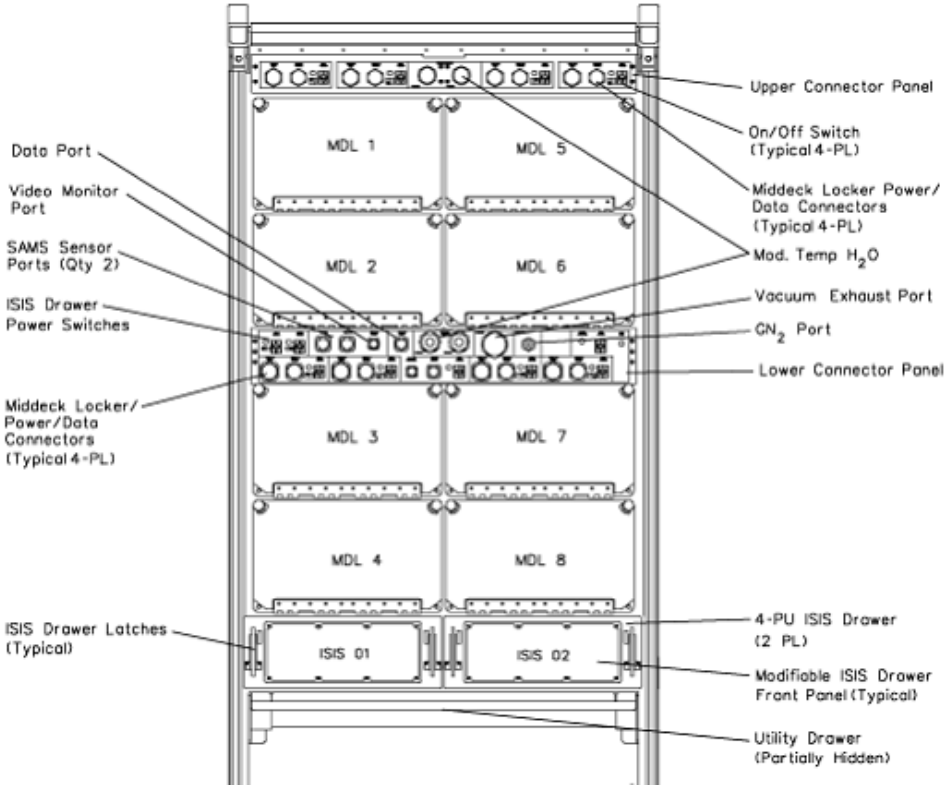

Figure 4-3 Example of an EXPRESS Rack (front view)

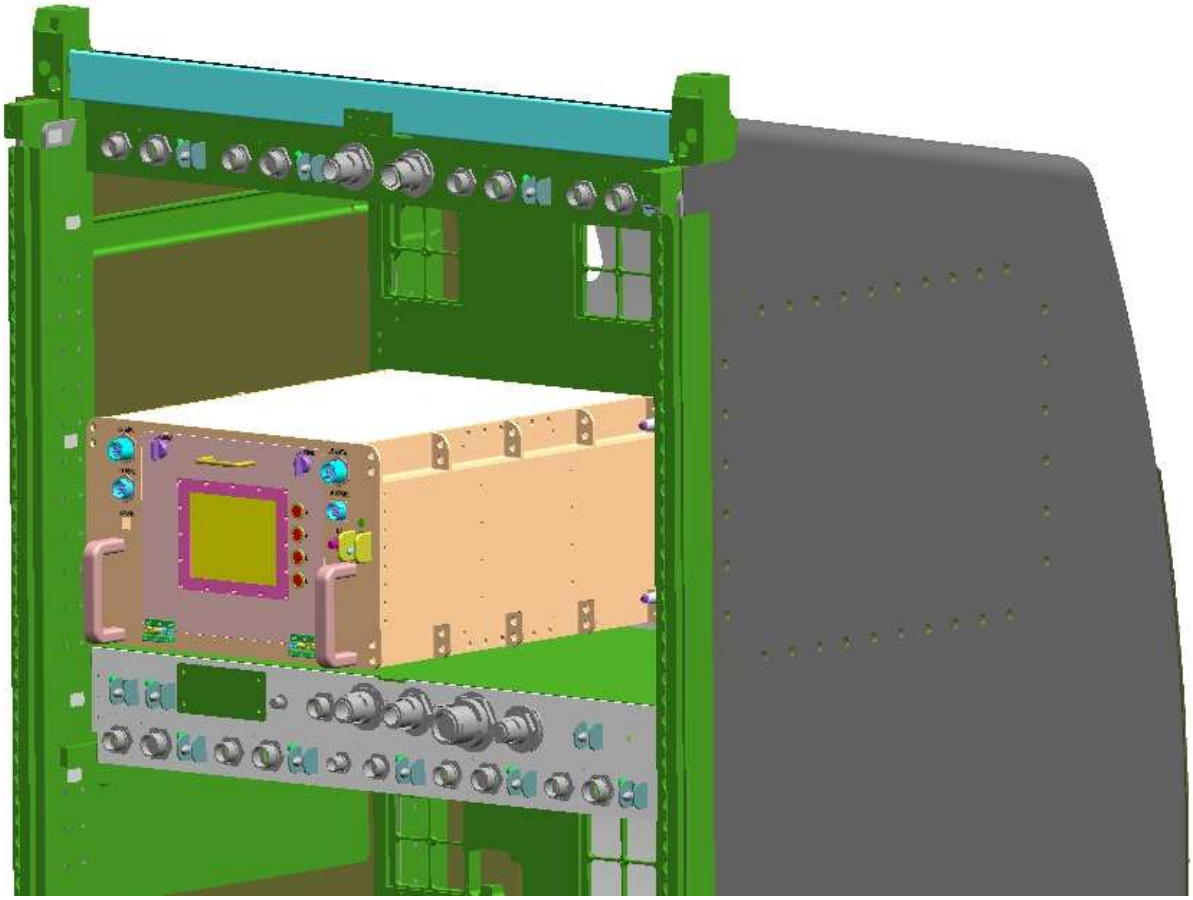

Figure 4-4 ACOP installed in an EXPRESS Rack (example of possible location)

ACOP provides these services:

1. On-orbit recording mechanism for large volumes of data at high rates
2. Play back for downlink of the recorded data at high rates
3. A crew interface for complex experiments
4. General computing facilities
5. Alternate bi-directional commanding path via the HRDL interface

ACOP will initially support a state-of-the-art particle physics detector, the Alpha Magnetic Spectrometer (AMS-02) experiment. AMS-02 uses the unique environment of space to study the properties and origin of cosmic particles and nuclei including antimatter and dark matter, to study the actual origin of the universe and potentially to discover antimatter stars and galaxies.

After the AMS-02 experiment, ACOP will remain in the US Lab as a general use computer for recording and managing large data volumes on the ISS. It will also allow a flexible and extensible control and monitoring interface for future payloads and, by using the large buffering capacity (> 1 TB), it will improve the data communication between Earth and the Space Station.

In addition to the ACOP system itself, shown in Figure 4-5 and Figure 4-6, a stowage bag will be sent to ISS with additional hard drives that can be exchanged with the hard drives in ACOP. From time to time the astronauts will perform this exchange enabling ACOP to record all of the AMS-02 data onto fresh hard drives. Once recorded, data will not be overwritten; rather the hard drives will be transported to ground as a permanent archive. The stowage bag will also contain spare parts for ACOP.

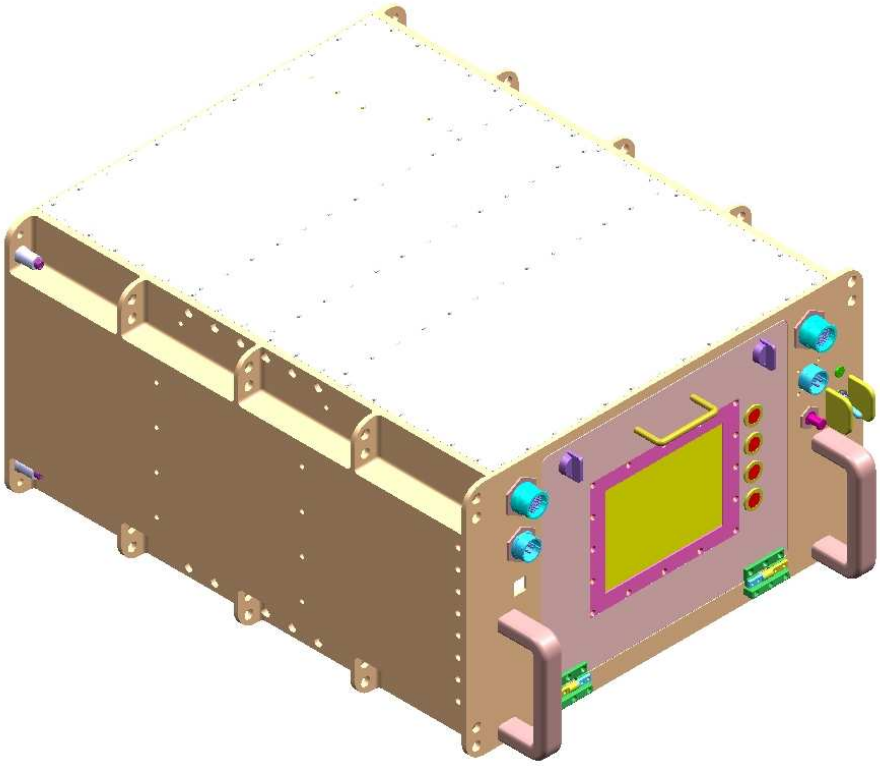

Figure 4-5 ACOP General Front View

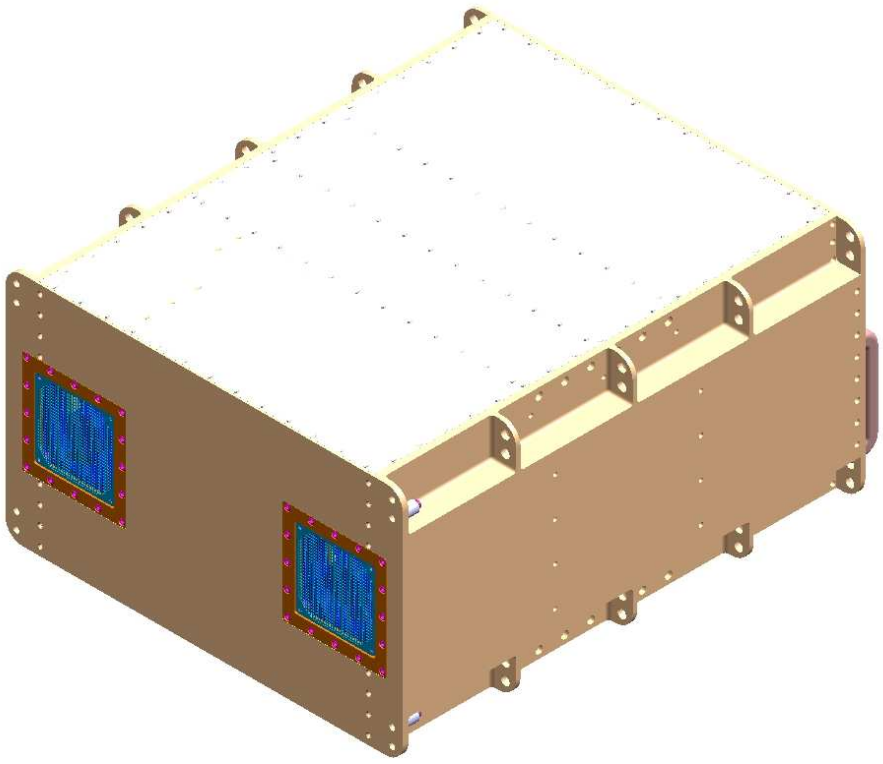

Figure 4-6 ACOP General Rear View

4.1 FUNCTION AND PURPOSE OF ACOP

ACOP has been designed to fulfill the requirements generated by the AMS-02 Collaboration. See the ACOP Common Design Requirements Document (document number: ACD-Requirements-Rev-BL, revision: baseline, date: September 2005) and the ACOP System Specification (document number: ACP-SY-CGS-001, issue: 3, date: March 2005) for a detailed description of the requirements.

The main characteristics of ACOP are summarized here below:

Capacities

1. Operates effectively in the ISS space environment.
2. Creates, on-orbit, an archive of all AMS-02 science data on removable and transportable media, using high capacity (200 GB or more) SATA hard drives.
3. Provides (based on an average data rate of 2Mbit/s) at least 20 days of recording capacity without crew intervention[1].
4. Provides (based on an average data rate of 2Mbit/s) at least 120 days of on board recording media capacity within an additional single mid-deck locker equivalent soft sided storage unit[2].
5. Recorded data is an irreplaceable archive of science data. Once recorded, data will not be overwritten; rather the hard drives will be transported to ground as a permanent archive.

Rates

6. For recording ACOP supports an orbital average data rate of at least 4Mbit/s with bursts of up to 20Mbit/s[3].
7. Supports the playback of recorded data to ground systems at selectable data rates up to at least 20Mbit/s sustained while simultaneously recording at prescribed rates (per 6.).
8. Supports an alternate AMS-02 ground commanding and housekeeping report path via the HRDL interface.
9. Supports ACOP to AMS-02 commanding at selectable data rates up to at least 20Mbit/s sustained. No requirement for simultaneous recording or playback operations at higher rates.

Interfaces

10. Provides a continuous operations display of ad hoc AMS-02 data and ACOP status for the ISS crew to monitor, via a LCD on the front panel.
11. Provides a continuous means for the ISS crew to issue ad hoc commands immediately to ACOP and to AMS-02 (without the need to un-stow or attach external equipment), by using accessible push-buttons on the front panel.
12. Provides an exhaustive diagnostic, monitoring and operations environment via the EXPRESS laptop computer.

Form

13. Housed within an EXPRESS rack locker and based on a CompactPCI 6U form factor.
14. Crew serviceable for hardware upgrades and repairs.
15. Crew serviceable for software upgrades and repairs.
16. Upgradeable and expandable using COTS subsystems.
17. Provides support of ISS system upgrades (e.g. 100bt MRDL follow on systems).

---

[1] Data capacity is completely dependent on application implementation.

[2] See note 1.

[3] The AMS-02 experiment has been designed to meet its physics goals when producing data at an average rate of 2MBit/s. Data is produced continuously. However, the physics that will be measured is unknown, and so are the peak and average data rates − 2Mbit/s average is the best estimate. Within AMS-02 a four-fold redundant 1GByte buffer (JBU) is provide to smooth the data flow and to allow for short term (less than an hour) interruptions in the data output from AMS, for example when the hard disk drives are being swapped within ACOP. After any such interruption, the data rate capability in ACOP must be able to make up for the lost time while not falling behind on the fresh data. Therefore ACOP is able to process data at a rate of at least twice the average data rate from AMS, namely 4Mbit/s.

18. ACOP is to weigh less than 35.5 kg without disks (launch weight)[4].
19. ACOP to consume less than 200 W (at 28Vdc)[5]
20. Launch compatible with MLPM mounting and dynamics.

4.2 UTILIZATION CONCEPT

The following are the key points of the ACOP operational concept as it pertains to the AMS-02 mission:

- ACOP is principally a ground operated payload
- ACOP provides the mechanism for the crew to monitor and control AMS-02. Both front panel and EXPRESS Rack laptop based interfaces are supported.
- ACOP is powered and active whenever AMS-02 is active. Only short (< 8 hours) outages.
- ACOP has continuous direct access to two physical HRDL connections (1 Tx/Rx pair plus an additional Tx, via UIP J7 connectors in other racks). By means of these interfaces:
  a. maintains a continuous Tx/Rx connection via APS to AMS
  b. provides intermittent, schedulable Tx connection for downlink.

  The additional Tx connection may be replaced by connection to the upgraded 100BaseT MRDL, when available.
- The AMS-02 TX connection may be tee'd by the APS to the HRFM/KU for direct downlink.
- As KU access is available, ACOP will be commanded to use its additional TX connection to down link data. ACOP will have the ability to burst this transmission (~20Mbits/sec).
- All data transmitted by AMS-02 is recorded onto ACOP hard drives as a master copy of the AMS-02 science data.
- When ACOP has acknowledged that the data is recorded, AMS-02 can release that data from its buffers.
- The four installed hard drives will require periodic replacement by the ISS crew from the onboard stock of empty drives (30 minute operation about every 20 days)
- A batch of 20 hard drives provides at least 120 days of recording capacity.
- New batches of hard drives will be delivered to ISS and the original master copies of the AMS-02 data will be returned to earth.

[4] See ACOP Design Report for the actual mass budget

[5] See ACOP Design Report for the actual power budget

5. ELECTRICAL DESIGN

5.1 ISS AVIONICS ARCHITECTURE

The ISS Command & Data Handling (C&DH) of the ACOP and AMS-02 system is shown as Figure 5-1.

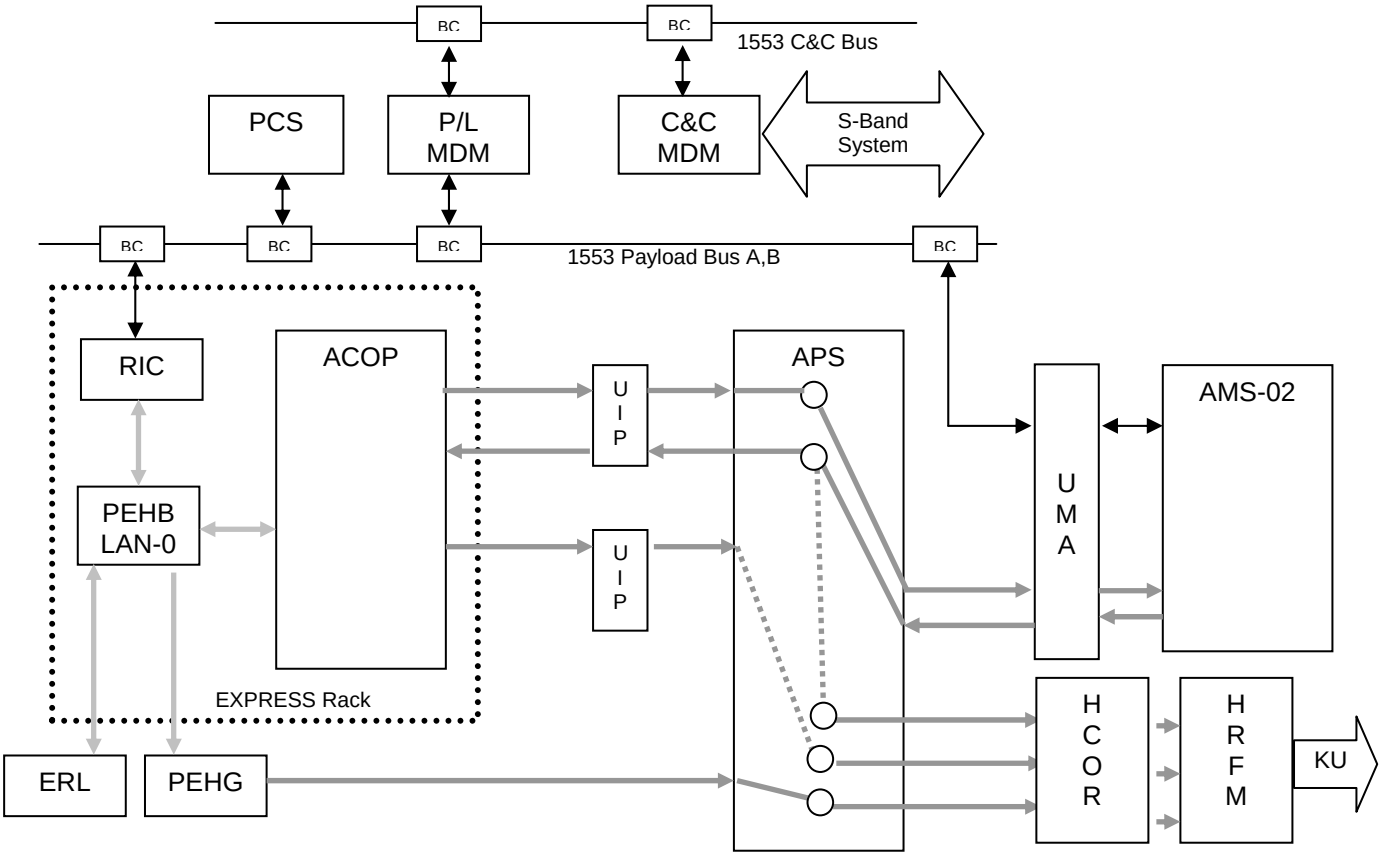

Figure 5-1 AMS-02 Avionics Architecture

Commanding and housekeeping data for ACOP is handled via the EXPRESS Rack Interface Controller (RIC). ACOP communicates with the RIC software on an Ethernet connection via the Payload Ethernet Hub Bridge (PEHB) using the Transmission Control Protocol/Internet Protocol (TCP/IP).

All ISS HRDL fibers are connected on one end to the Automated Payload Switch (APS). This device provides cross bar switching among the fiber systems of ISS. ACOP has two prime targets for HRDL transmission transfers. The first is the High Rate Frame Multiplexer (HRFM - via the High-Rate Communications Outage Recorder (HCOR). The HRFM interleaves data to the KU-Band transmission system for downlink. The second transmission target is the AMS-02 payload. The APS can be configured to tee data transmitted by AMS-02 to both the HRFM and ACOP. ACOP has a single receive source for HRDL which is the AMS-02 payload.

At all times ACOP maintains an active bi-directional connection via the HRDL interfaces to AMS-02. As KU access is made available, ACOP can be commanded to use its additional TX connection to down link data. ACOP will have the ability to burst this transmission (~20Mbits/sec). All data transmitted by AMS-02 is recorded onto ACOP's hard drives as a master copy of the AMS-02 science data. When ACOP has acknowledged that the data is recorded, AMS-02 can release that data from its buffers.

5.2 ACOP AVIONICS ARCHITECTURE

The ACOP system is based on CompactPCI systems. It contains a single board computer and several interface boards (including HRDL fiber interfaces, Ethernet interfaces, USB interfaces to upgrade the operating system and programs, digital input-output and video interfaces).

ACOP will also contain four exchangeable hard disks used to archive the data and the necessary interfaces. Other parts of ACOP are a LCD screen and a simple push button interface, present on the ACOP Front Panel as part of the man-machine interface.

Fans will guarantee the internal air flow necessary for cooling. A thermal sensor network will be mounted on the chassis and PCBs to monitor the operating temperatures.

In the main chassis and front panel there are the electrical parts which include a set of digital computer hardware and software. The functional block diagram of electrical parts is shown as Figure 5-2.

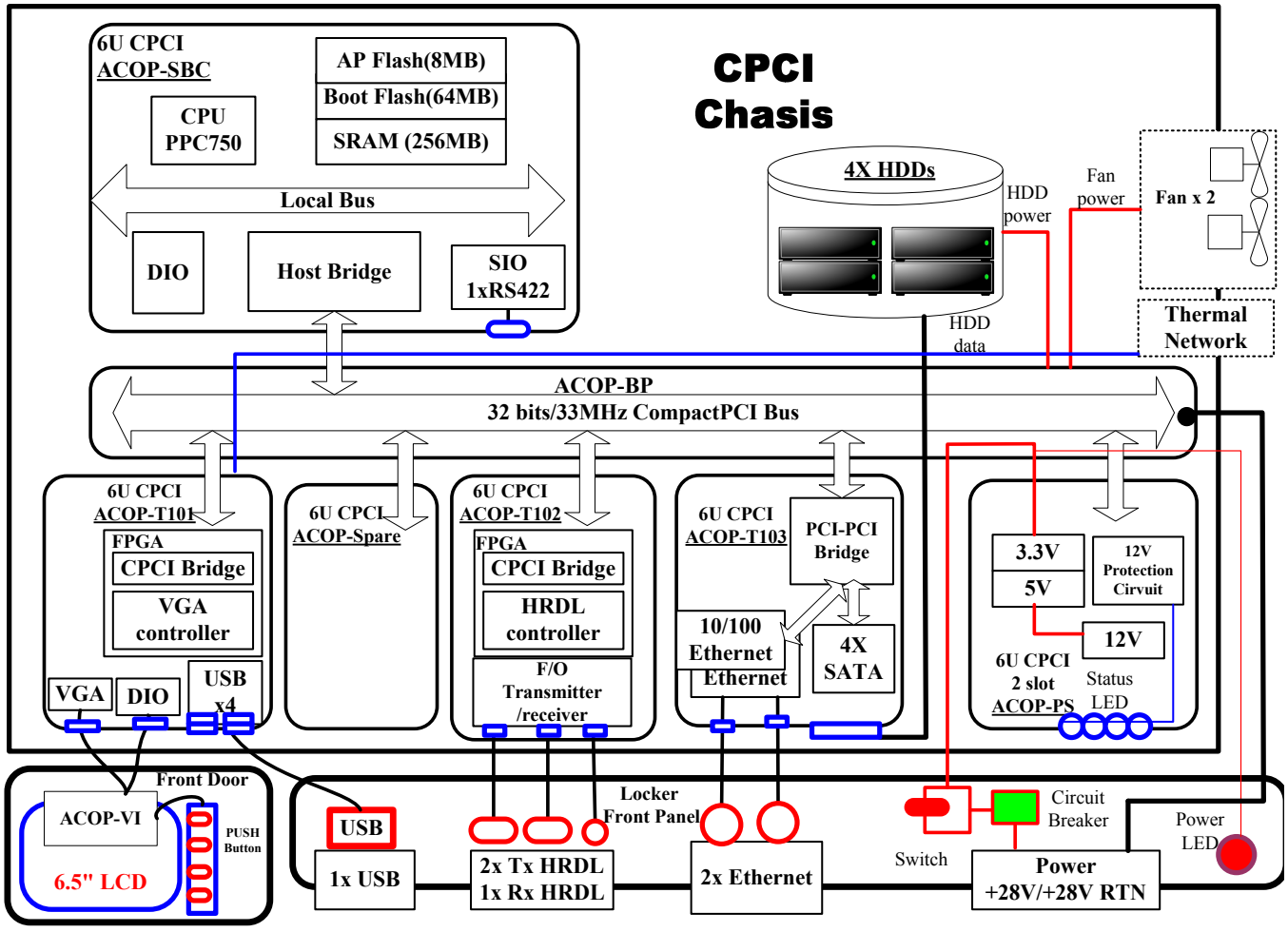

Figure 5-2 ACOP Electrical Block Diagram

The ACOP chassis includes the following modules:

- ACOP-SBC: single board computer, based on the IBM PPC 750, which provides 400Mhz speed as well as standard CompactPCI bus interfaces and acts as CompactPCI system slot.
- ACOP-T101: provides video output interface, 4 USB 2.0 interfaces, and a digital I/O (DIO) interface.
- ACOP-T102: provides 2 fiber optic transmit and 1 fiber optic receive interfaces.
- ACOP-T103: provides 2 Ethernet ports and 4 SATA ports.

- ACOP-Spare: spare slot for future expansion purpose
- ACOP-PS: double height power supply.
- 4 hard disk drives mounted in exchangeable caddies

The ACOP front panel will be equipped with:

- One aircraft style push button Circuit Breaker
- Four Momentary Push Buttons
- One On/Off Toggle Switch
- One LED monitoring power supply presence (Power Status LED)
- One HRDL Connector
- One Power Connector
- Two MRDL Connector with 10/100 base Ethernet
- One USB connector
- One LCD screen with LED backlight

5.2.1 POWER DISTRIBUTION AND POWER FEEDERS PROTECTIONS

The ACOP power distribution system includes the power input control on the locker front panel, the power distribution in ACOP backplane (ACOP-BP) and the power supply (ACOP-PS) module, as shown in Figure 5-3.

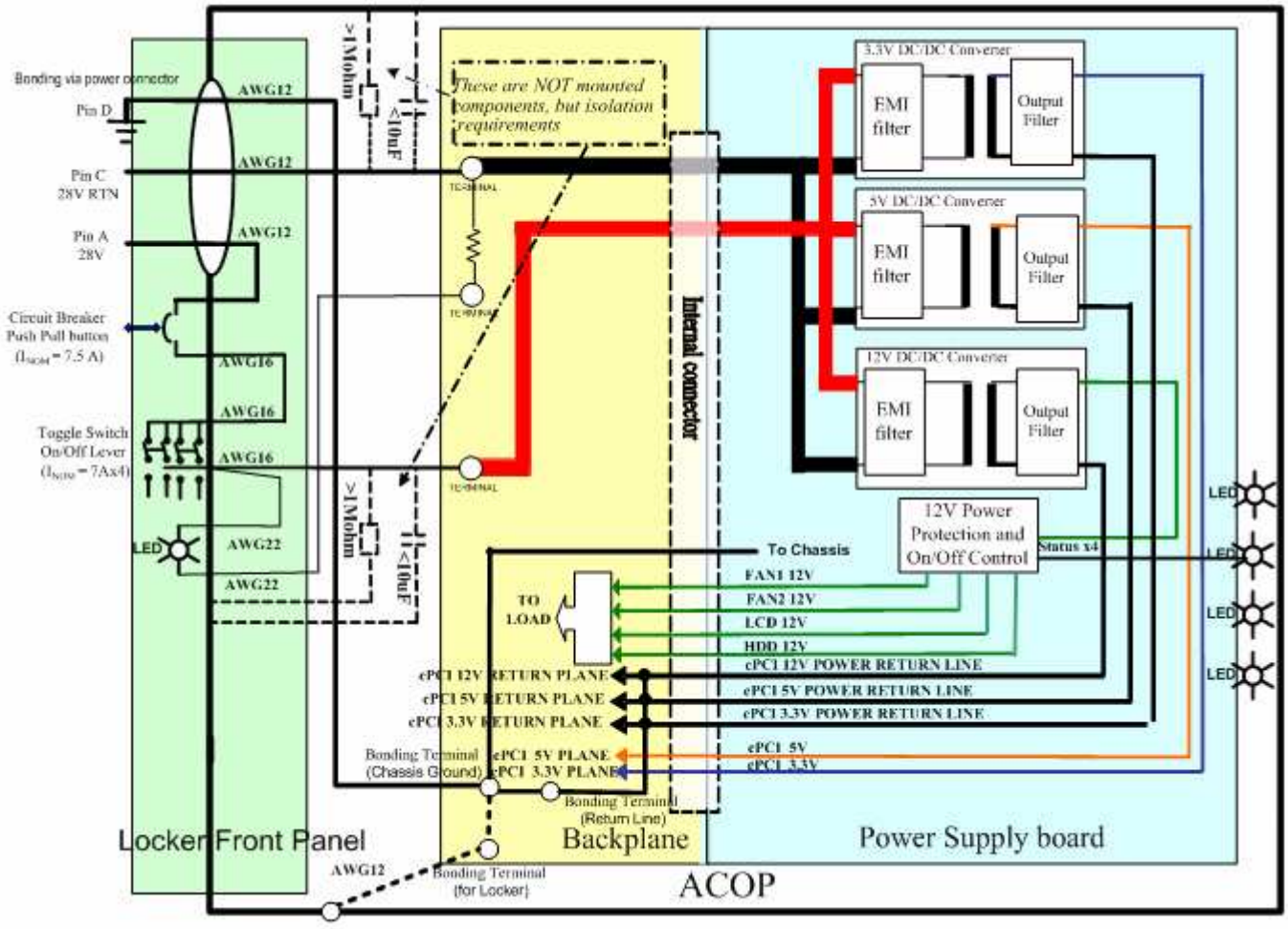

Figure 5-3 ACOP Power Distribution Diagram

The input voltage range for ACOP is 24 to 32Vdc, compliant with the +28Vdc power feeder voltage range provided by the EXPRESS Rack. The input voltage is first supplied to a circuit breaker which is used to protect wirings and downstream circuits from thermal damage that occurs during an over-current situation and as the first step of defense against electrical hazards. The circuit breaker's features include fail-safe operation, ambient temperature compensation and load protection function.

When not tripped the circuit breaker provides power to the front panel power switch. When the switch is moved to the ON position, power is provided to the system and a LED is turned on to indicate presence of 28V input voltage.

The switch output supplies the ACOP Power Supply (ACOP-PS), which is based on modular DC/DC converters implemented with hybrid integrated circuits. Each one incorporates two filters designed with output common mode filter chokes and low ESR capacitors. Three outputs provide 3.3Vdc, 5Vdc and 12Vdc power supplies with independent output regulation.
There are power terminals on ACOP-BP for distribution of regulated power to other ACOP devices. The DC-DC converters in ACOP-PS include a complete self contained EMI filter, allowing these units to meet MIL-STD-461 levels. Additional features include output common mode filtering, programmable soft start, open loop OVP protection, external synchronization inputs and an inhibit input.

The three different voltages, 3.3V, 5V and 12V, are distributed through the ACOP backplane from the ACOP-PS to the CompactPCI boards and other stand-alone devices (LCD, fans, etc.). There are protection circuits for each 12V power distribution, and the status is indicated by board mounted LEDs.

5.2.1.1 POWER INPUT CONTROL

The ACOP Locker front panel power input control includes the following functions:

- *4 pole On/Off Toggle Switch*

  This part (M8805/93-012) has been selected to meet the maximum input current requirement, including the condition of HDD startup with all 4 HDDs on simultaneously. Four poles of the switch are used, and connected in parallel. The current rating is 7A X 4 for 4 poles.
- *LED to indicate Power ON/OFF status*

  A green LED (JANTXM19500/521) is mounted on the Locker front panel to indicate Power ON/OFF status. A resistor (mounted on ACOP-BP) is connected in series to this LED to limit its current.
- *Aircraft style push button Circuit Breaker for input over current protection*

  The estimated maximum input power of ACOP is 113.45W (not including circuit breaker and wire losses). The estimated minimum input voltage of DC/DC Converters is:

  24V (Vin lower bound) – 0.3V (CB voltage drop) – 0.2V (Wire loss drop) = 23.5V.

  Therefore, the maximum input current is Pin(max) / Vin(min) = 113.45 / 23.5V = 4.83A. A 7.5A Circuit Breaker (MS 3320-7 1/2) has been selected to meet the requirements.

5.2.1.2 POWER SUPPLY MODULE

The ACOP-PS module is CompactPCI form factor, installed in the ACOP backplane, and provides the power source for ACOP electronics parts. The ACOP-PS includes the following functions (for details see Para. 5.8):

- Convert input power (DC 28V) to meet the power requirements of all ACOP electronics parts.
- Isolation between 28V input from ISS and output load.
- Protection of each power output (3.3V, 5V, 12V)
- 3.3V and 5V power source with a function of remote sensing.
- Provide on/off control of each 12V power distribution to Fan1, Fan2, and LCD.
- Provide protection status of each 12V power distribution to system, and indicate by board mounted LEDs.
- Provide two Dallas thermal sensors for each DC/DC Converter.

5.2.2 POWER-ON SEQUENCING

The ACOP-SBC board will provide a power monitor circuit for both the 3.3V and 5V supplies: during power up, the 3.3V power monitor circuit will hold the ACOP-SBC in reset until the power is stable. The 5V power monitor signal will be latched when faulted and the latched result will be provided as input to the CPU for software read and then clear operation.

5.2.3 ACOP INTERNAL LAYOUT

Figure 5-4 shows the internal layout of boards and components inside ACOP as it will be seen by the crew when the front panel is open.

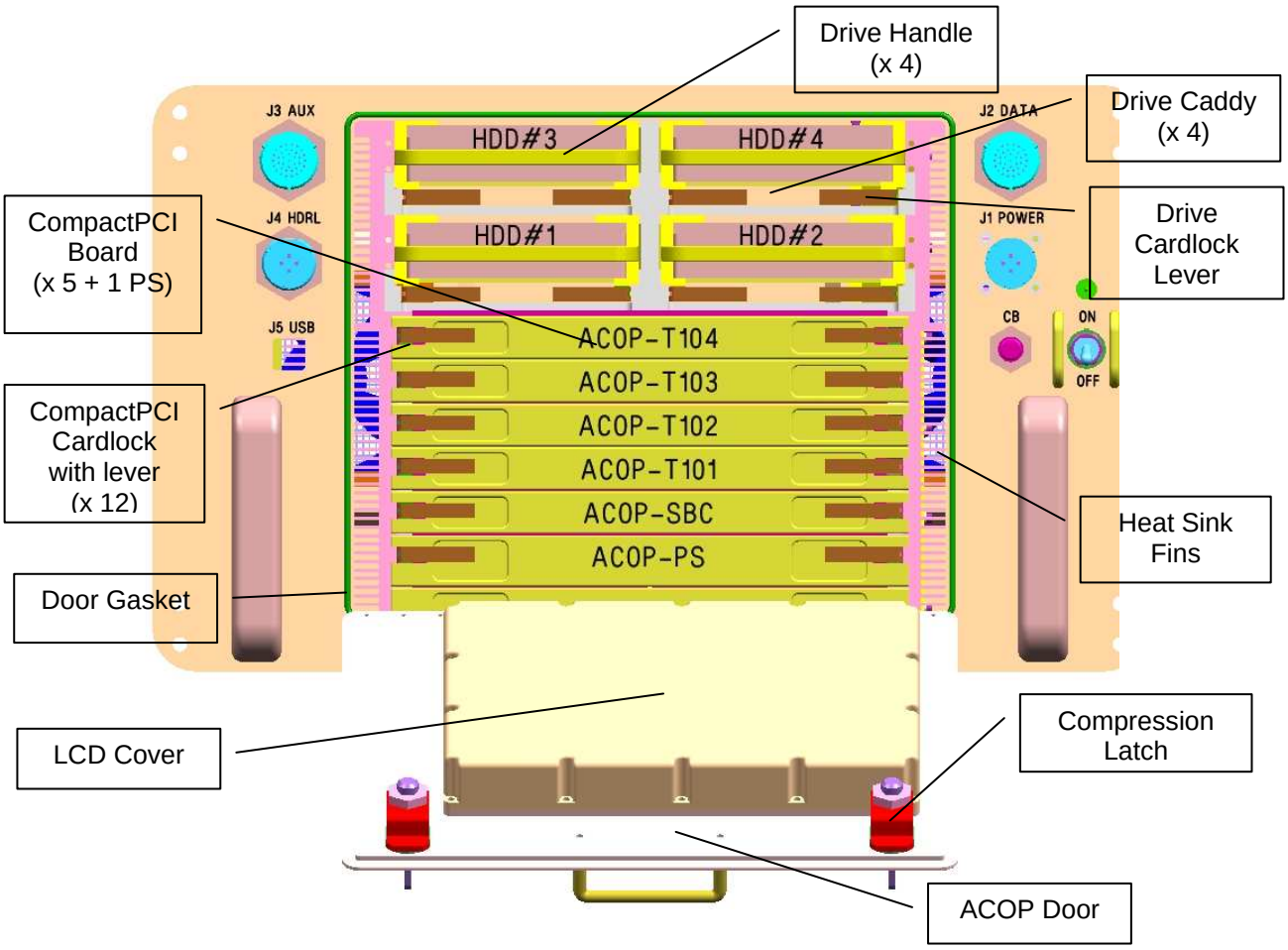

Figure 5-4 ACOP Main Components

The upper part of the chassis will be occupied by 4 Drive Caddies holding Serial ATA hard drives. The Drive Caddies will be fixed to the chassis by means of cardlock retainers provisioned with lever arms to minimize the crew effort to replace them. Power and data interface to each Drive Caddy is provided by means of a blind mate connector placed on the rear side.

The CompactPCI boards and the power board will be hosted in the lower section of the chassis. These boards will also be fixed to the chassis by means of cardlock retainers.

The main characteristics of the ACOP chassis assembly are:

- 6U card cage for 5 double Eurocard CompactPCI boards.
- Conduction cooling and wedge-locks for CompactPCI boards and power supply board.
- Double height power supply slot.
- Mounting provisions for CompactPCI backplane.
- 4 hard drives with caddies that can be removed from the chassis

The CompactPCI bus combines the performance advantages of the PCI desktop architecture with the ruggedness of the Eurocard form factor, a widely used standard within the industry for over 20 years. The Eurocard board provides more secure connectors and more available space for professional embedded platforms than the PCI cards in desktop computers. The CompactPCI standard has widely been accepted for a large spectrum of applications.

5.2.4 ACOP CCA (CARD CAGE ASSEMBLY) DESIGN

The CCA design in the ACOP case is based on the “IEEE 1101.2 - Mechanical Core Specification for Conduction Cooled Eurocards” specification and the board layout is shown in Figure 5-5:

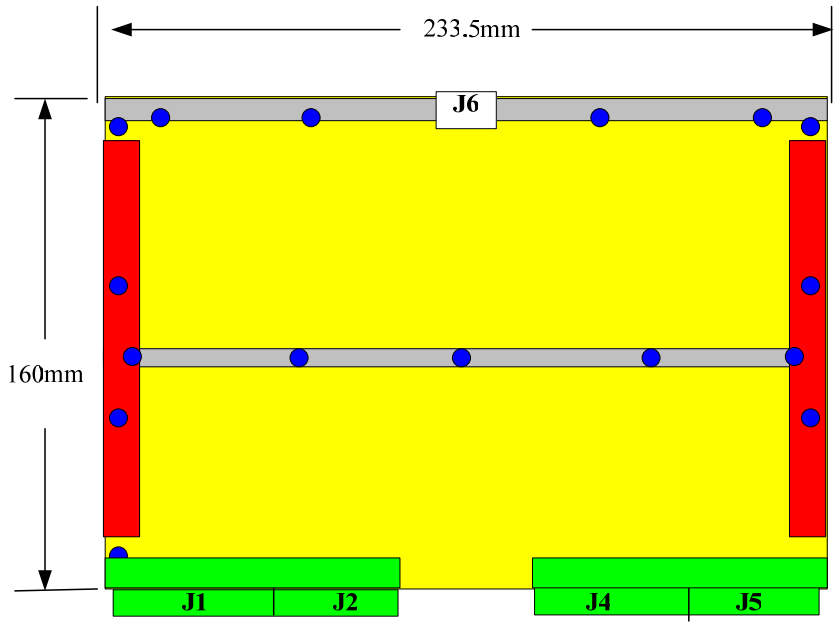

Figure 5-5 IEEE 1101.2 - Mechanical Core Specification for Conduction Cooled Eurocards

To allow ACOP to operate in the ISS, the boards design incorporates the following techniques:

- Buried thermal layers within the PCB and provide a good thermal conductivity from components to the board edge.
- Heat sink for high power components
- Stiffening ribs cross the board
- Expandable wedge lock on both sides
- Components location based on thermal analysis

Material, finished board dimensions and mass budget of all CCAs are reported in the following two tables:

	ACOP-SBC	ACOP-T101	ACOP-T102	ACOP-T103	ACOP-T104	ACOP-BP	ACOP-PS	ACOP-VI
Material	Polymide (85N)	Polymide (85N)	Polymide (85N)	Polymide (85N)	Polymide (85N)	Polymide (85N)	Polymide (85N)	Polymide (85N)
Board thickness (mm)	1.6	1.6	1.6	1.6	1.6	3.0	1.6 (TBC)	1.6 (TBC)
Board dimensions (mm)	160x233.35	160x233.35	160x233.35	160x233.35	160x233.35	141.24x262.05	160x233.35	120.36x158

Table 5-1 ACOP PCB Specifications

PCB Board	Mass Budget (grams)	Contingency [%]
ACOP-SBC	400	5%
ACOP-T101	350	5%
ACOP-T102	350	5%
ACOP-T103	350	5%
ACOP-T104	TBD	---
ACOP-BP	220	10%
ACOP-PS	1000	10%
ACOP-VI	TBD	---

Table 5-2 ACOP PCB Mass Budget

5.3 ACOP-SBC

The ACOP-SBC is a single slot 6U CompactPCI form-factor board that fits into a system slot of a standard CompactPCI backplane. It consists of an IBM PowerPC750 CPU with system memory, several peripherals and the CompactPCI interface.

Figure 5-6 shows the main functional blocks that make up the ACOP-SBC board. There are two bus sections in the ACOP-SBC board design: the CPU bus provides connections to the North PCI Bus Bridge chip, which provides the connections to the processor memory.

The processor memory includes read only boot PROM, FLASH memory and SDRAM. The system allows the operational memory configuration to be customized to the specific application.

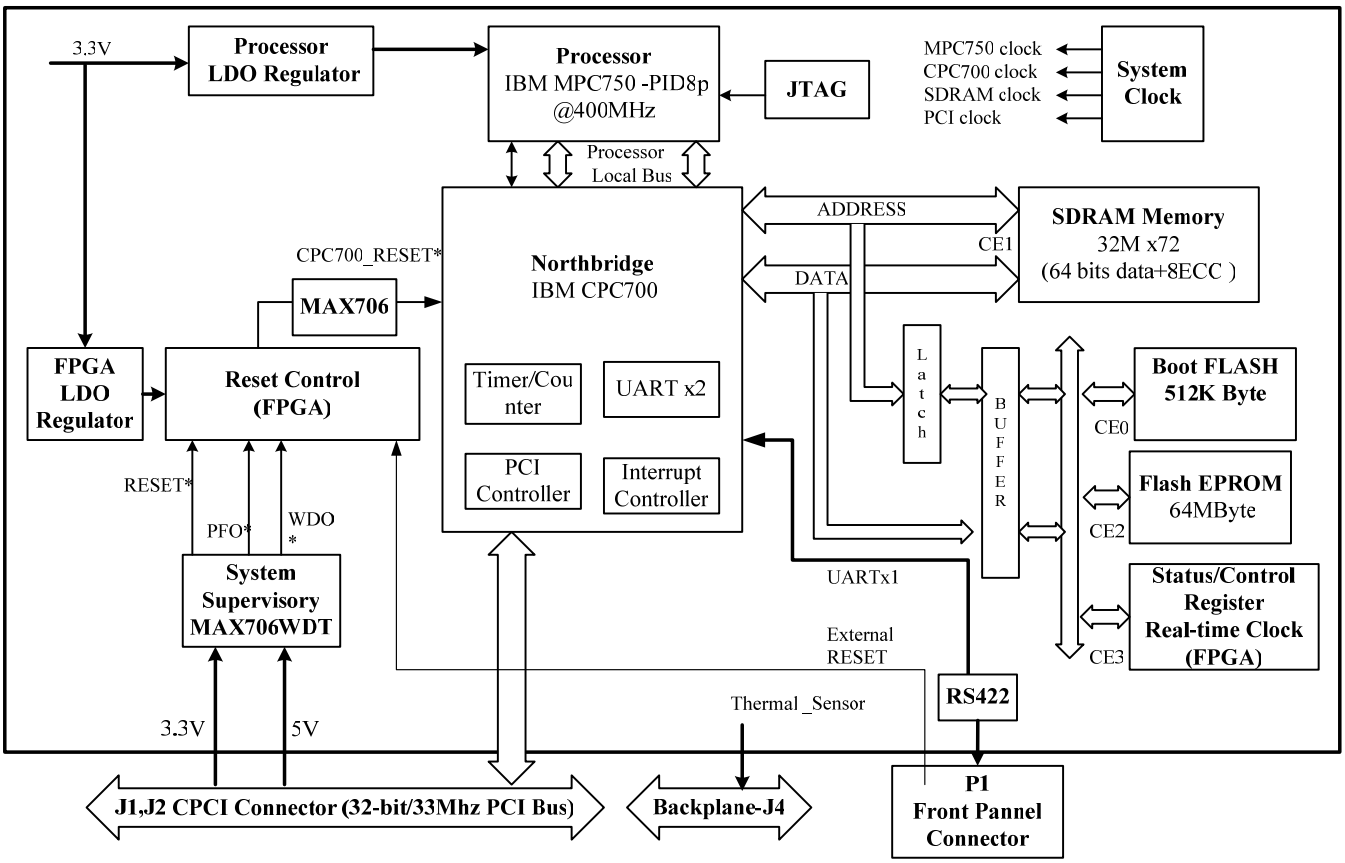

Figure 5-6 ACOP-SBC Functional Block Diagram

5.3.1 ACOP-SBC FEATURES

The following is a list of the hardware features for the ACOP-SBC:

- Microprocessor
  IBM PowerPC750 microprocessor running at 400 MHz
  On-chip Cache (Instruction/Data): 32K/32K

- CPU to PCI Bridge
  IBM CPC700 memory controller and PCI bridge
  CPU to SDRAM/ROM/Peripheral controller
  CPU to PCI bridge

PCI to SDRAM bridge
Provides Backplane CompactPCI signal

- Memory
  Boot PROM: 512K bytes Flash EEPROM
  Flash EPROM: 8M bytes, 32-bits wide
  SDRAM: 256M bytes, data bus width 72-bits with 64 bits data and 8 bits ECC

- 12 external interrupts, individually maskable

- Watchdog timer and supervisory circuit
  Power-on-reset, external reset
  Timer to monitor the CPU operation
  Power supply monitor for +3V and +5V

- On-board Peripheral
  Serial I/O: 16552D (16550A compatible), RS422 Interface
  General purpose timer: 32-bits time base, 5 capture event timers and 5 compare timers
  Control register: Control/status registers, Watchdog restart/read, enable/disable register
  Real-time clock count to mini-second

- Two set vias (three wires x 2) for thermal meters input

- PCI 2.1, 32-bits, 33Mhz, with 5 bus arbiter (REQ/GNT signal)

- CompactPCI system slot, PICMG 2.0 compliant

5.3.2 ACOP-SBC PERFORMANCE

- PCI bus transfer rate
  A total of 64 bytes pre-fetch buffer allows pre-fetch data to maximize burst throughput of PCI bus

- CPU to SDRAM
  Max. 32bytes burst transfer cycles

- Processor compute performance : processor frequency at 400MHz
  Estimate peak performance: 733 MIPS
  SPECint95 18.8
  SPECfp95 12.2

- Board operating frequency
  CPU running at 400MHz
  PLB (Processor Local Bus) bus clock 66MHz
  SDRAM clock 66MHz

5.3.3 ACOP-SBC HARDWARE DESIGN

5.3.3.1 MICROPROCESSOR

The ACOP-SBC computer board utilized an IBM MPC750 microprocessor running to a peak of 400MHz. The MPC750 is an implementation of the PowerPC microprocessor family of reduced instruction set computer (RISC) microprocessors. The MPC750 implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16, and 32bits, and floating-point data types of 32 and 64 bits. The MPC750 has independent on-chip, 32-Kbyte, eight-way set-associative, physically addressed caches for instructions and data and independent instruction and data memory management units (MMUs). The MPC750 has a processor local bus (PLB bus) with 32-bit address bus and 64-bit data bus to access external devices.

There is a JTAG port for a in-circuit emulator unit to be used during board debug.

5.3.3.2 SDRAM

256M bytes of SDRAM are available for program data storage and execution. The memory devices used in this design are organized as 32M x72 in order to provide 64 bits data bus and 8 bits ECC code.

In general, the ECC is single error correcting / double error detecting (SEC/DED). The SDRAM can be accessed 8, 16, 32 or 64 bits at a time. The ECC can also detect 3/4 bit errors within a nibble (data bits 0~3, data bits 4~7, etc.) as an uncorrectable error. Multi-bit (3 or more) errors spread across multiple nibbles cannot be handled.

Any write access smaller than 64 bits at a time will incur a large speed penalty. When ECC is enabled the ECC controller will convert all writes that are less than 8 bytes to a read-modify-write for the memory access to preserve the ECC encoding on the entire double word (as is required).

5.3.3.3 FLASH EEPROM

The Flash memory is 64MBytes organized as 16M by 32 bits. The flash memory is used to store the RTOS code and the application code. The flash memory will support execution of instructions without copying to SDRAM; however copying to SDRAM will increase execution performance. The flash memory can be programmed in-system with the standard system 3.3V VCC supply, it has a limited erase cycle of 1,000,000 Program/Erase Cycles and 20 Year Data Retention period.

5.3.3.4 BOOT FLASH ROM

ACOP-SBC provides up to 512K bytes boot Flash ROM. The boot PROM is used for booting the ACOP-SBC board. During cold start or reset condition, the program counter of CPU is point to boot PROM such that CPU can fetch and execute the code from boot PROM. The access method of boot PROM is an 8 bits non-burst operation.

5.3.3.5 UART

There are two 16550 compatible UARTs with two 2-wire serial interface allowing a maximum baud rate connection each of 56000 bps. These are for debugging and control. The UARTs can be put into FIFO mode to relieve the processor of excessive software over-head. Here internal FIFOs are activated, allowing 16 bytes (plus three bits per byte of error data in the RCVR FIFO) to be stored in both receive and transmit modes. The timing reference clock is the CPC700 System clock input divided by 4. One of the UARTs will be converted to RS422 signal level and connected to a 9 pins micro D-type connector mounted on the front panel of the ACOP-SBC board.

5.3.3.6 TIMER/COUNTER

The timer/counter function includes a 32-bit time base counter and ten 32-bit timers, five capture timers and five compare timers. These timers can be set by the application program to separate time base counter or system timer.

The time base counter provides the reference time for all capture and compare timers and continually increments once every System clock unless written or reset.

Each of the five capture timers is 32 bits wide and captures the time base counter value. Whenever a capture event is generated, if the corresponding interrupt enable register bit is set, the interrupt will be sent to the CPC700 interrupt controller. If enabled in the CPC700 interrupt controller, the capture event can be used to interrupt the processor.

Each of the five compare timers is 32 bits wide and provides a reference value which is compared to the time base counter. The compare timer continually compares its 32-bit programmed value with the time base counter value on a bit by bit basis. If the corresponding interrupt enable register bit is set, the interrupt will be sent to the CPC700 interrupt controller. If enabled in the CPC700 interrupt controller, the compare event can be used to interrupt the processor.

The timers/counters function is contained within the CPC700 Bridge Chip.

5.3.3.7 INTERRUPT CONTROLLER

The Interrupt Controller provides control of 29 interrupt sources including:

- 12 External Interrupts
- 10 Timer interrupts - 5 Compare and 5 Event Capture
- 2 UART interrupts
- 2 IIC Interrupts
- PCI write to CPC700 PCI Command Register interrupt
- PCI write to specific local memory range interrupt
- ECC correctable error interrupt
- These interrupts are individually maskable and interrupt types and polarity are programmable.

The mapping of external interrupt sources to the interrupt controller is as follow:

- INT3: PCI INTA* from backplane
- INT4: PCI INTB* from backplane
- INT5: PCI INTC* from backplane
- INT6: PCI INTD* from backplane

The interrupt controller is implemented in the CPC700 Bridge Chip .

5.3.3.8 SYSTEM CLOCK

All clock sources in ACOP-SBC is generated by MPC792 device. The frequency of PPC750 and SDRAM clock is set to 66.6MHz. The CPC700 and PCI clock is one half the frequency and in phase with the PPC750 processor and SDRAM clocks. PCI Bus Interface is configured to operate synchronously to the processor bus.

5.3.3.9 GENERAL-PURPOSE REGISTERS

There are six general-purpose registers are used to control and monitor a variety of functions. They are all 8 bits width and locate at memory bank 3. Four of the registers are read/write capable and allow the use of AND or OR instructions to clear and set individual bits. The other two are read only.

5.3.3.10 SYSTEM SUPERVISORY

The ACOP-SBC board supports several methods to reset the board for space application. There are following reset sources:

- Cold star or under voltage resets from the voltage supervisor
- External reset input via front panel connector
- Watchdog timer (WDT) timeout

The watchdog timer function (WDT) is provided to monitor the operation of the ACOP-SBC computer board. If for some reason, the microprocessor cannot strobe the watchdog timer input within a specified period of time, the WDT will issue a reset pulse to the processor.

The voltage monitor sense both the 3.3V and 5V supply input, both the status signal will be latched in control/status register (Power_ON_Detect bit for 3.3V and 5V_Power_Good bit for 5V). This reregister can be read and clear by CPU. When 3.3V power is first applied to ACOP-SBC or when 3.3V power level is below 3.0V, the power monitor circuit will assert a reset pulse to the processor.

5.3.3.11 REAL TIME CLOCK

ACOP-SBC supports a real time clock to record the duration after system power-on. The real time clock function includes two groups of counting registers for milliseconds and seconds. All register can be latched and read back by CPU. The real time clock function also includes a reset register, when CPU performs a write operation to this register will clear all the counting registers. The real time clock function is implemented within FPGA.

5.3.3.12 ADDRESS MAP AND CONFIGURATION

During power-up the boot ROM will automatically assigns the addresses and configuration based on the requirements of each device. Since the hardware configuration of ACOP-SBC is fixed, the assigned address is also determined. The addresses and configuration will be set as follow (see next page).

A more detail description of address map is as following:

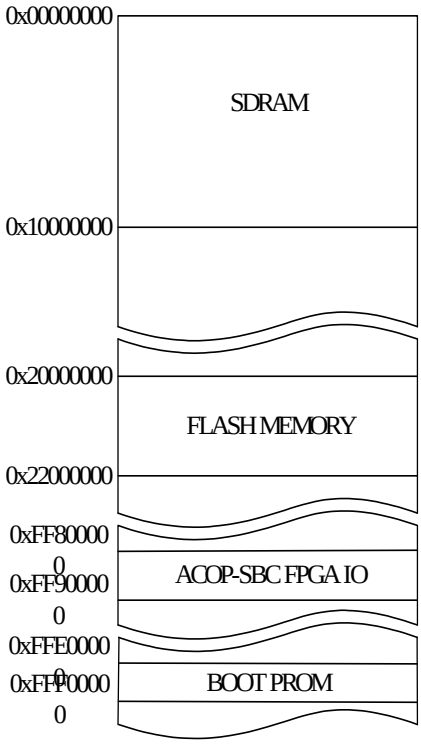

Figure 5-7 ACOP-SBC Memory Map

- **Local Memory Address Map-Processor View**

The CPC700 incorporates a simple fixed processor address map that serves the PowerPC processor. The address map has provisions for ROM, SDRAM, flash, peripheral I/O and PCI interface. The range of addresses is defined by the address map detailed in the following table:

Processor Address Range		Description
0 to 2G-1	h00000000 h7FFFFFFF	System Memory Typically reserved for local memory
2G to 4G-11M-1	h80000000 hFF4FFFFF	PCI Interface
4G-11M to 4G-10M-1	hFF500000 hFF5FFFFF	DCR – Configuration Address/Data
4G-8M to 4G-8M-1	hFF600000 hFF7FFFFF	Internal Peripherals
4G-8M to 4G-2M-1	hFF800000 hFFDFFFFF	System control/status registers
4G-2M to 4G-1	hFFE00000 hFFFFFFFF	System Boot ROM

Table 5-3 ACOP-SBC Local Memory Map

- **PCI Core Space Address Map – Processor View**

The address range of PCI core space is from 80000000h to FF4FFFFFh. There are three local windows available to the PowerPC to access PCI memory. These windows can be programmed to powers of 2 boundaries, are variable in size, and may be used to access any location in a 64-bit PCI address space yet are invisible to the PCI bus. PCI local memory access is handled in the PCI standard method, through the programming of the Base Address Registers (BARs) in PCI configuration space. These registers are defined to allow the PowerPC processor to request allocation of resources on the PCI side.

Description	Stating address	End address	Range
	8000 0000	FF4F FFFF	2GB-11GB
PCI memory	8000 0000	F7FF FFFF	
PCI I/O	F800 0000	F800 FFFF	
Reserved	F801 0000	F87F FFFF	
PCI I/O	F880 0000	FBFF FFFF	
Reserved	FC00 0000	FEBF FFFF	
PCI Configuration register	FEC0 0000	FEC0 0004	
PCI Interrupt Acknowledge	FED0 0000	FEDF FFFF	
Reserved	FEE0 0000	FF3F FFFF	
PCI local Configuration Registers	FF40 0000	FF40 003C	

Table 5-4 PCI Core Space Address Map

- **ACOP-SBC Local Memory Address Map – PCI View**

There are three local windows available to the PCI master to access Local memory. These windows can be programmed to powers of 2 boundaries, are variable in size, and may be used to access any location in a 64-bit ACOP-SBC local address space.

PLB Address Range		Description
0 To 2G-1	h00000000 h7FFFFFFF	System Memory PCI accesses to this range will target system memory and be snooped. Snooping can be disabled for a particular region using the PRIFOPT1, PLBSNSSA0, PLBSNSEA0 registers.
2G to 4G-2M-1	h80000000 hFFDFFFFF	Reserved The processor interface does not respond to accesses in this range.
4G-2M to 4G-1	hFFE00000 hFFFFFFFF	System Memory(Boot ROM) PCI accesses to this range will target system memory and be snooped. Snooping can be disabled for particular region using the PRIFOPT1, PLBSNSSA0, PLBSNSEA0 registers.

Table 5-5 ACOP-SBC Local Memory Address Map – PCI View

5.3.3.13 CompactPCI Bus Interface

The ACOP-SBC is designed to meet the CompactPCI interface standard. For the PCI interface operation, the CPC700 chip provides a mechanism for connecting PCI devices to the local PowerPC processor and local memory. This interface is fully compliant with version 2.1 of the PCI Specification and includes a 32 bit PCI data bus path, bus arbiter and interrupt control.

Mostly electrical design meet the CompactPCI electrical requirement for system slot such as stub termination, clock signal, signals pull-up resistors, REQ#/GNT# signals. Compatibility will be provided with standard CompactPCI backplane as well.

5.3.3.14 External Interfaces

The ACOP-SBC includes the following external interfaces:

- J1 (To ACOP Backplane): includes standard CompactPCI 32bits/32Mhz J1 signals

25	GND	5V	Pull-up	Pull-up	3.3V	5V	GND
24	GND	AD[1]	5V	N.C.	AD[0]	Pull-up	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	Pull-up	C/BE[0]#	GND
20	GND	AD[12]	GND	N.C.	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	N.C.	N.C.	GND	PERR#	GND
16	GND	DEVSEL#	GND	N.C.	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	KEY AREA						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	N.C.	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	N.C.	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ0#	GND	3.3V	Pull-up	AD[31]	GND
5	GND	N.C.	N.C.	RST#	GND	GNT0#	GND
4	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	N.C.	5V	N.C.	N.C.	N.C.	GND
1	GND	5V	-12V	N.C.	+12V	5V	GND
Pin	Z	A	B	C	D	E	F

Table 5-6 ACOP-SBC J1 Pin Function

- J2 (To ACOP Backplane): includes standard CompactPCI 32bits/32Mhz J2 signals

22	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
21	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
20	GND	N.C.	GND	N.C.	GND	N.C.	GND
19	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
18	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
17	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
16	GND	N.C.	N.C.	N.C.	GND	N.C.	GND

15	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
14	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
13	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
12	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
11	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
10	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
9	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
8	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
7	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
6	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
5	GND	N.C.	GND	N.C.	N.C.	N.C.	GND
4	GND	N.C.	N.C.	N.C.	GND	N.C.	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin	Z	A	B	C	D	E	F

Table 5-7 ACOP-SBC J2 Pin Function

- J4 (To ACOP Backplane): includes peripheral input/output signals

25	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
24	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
23	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
22	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
21	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
20	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
19	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
18	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
17	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
16	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
15	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
12-14	KEY AREA						
11	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
10	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
9	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
8	GND	CHA_GND.[6]	N.C.	N.C.	N.C.	N.C.	GND
7	GND	CHA_GND.[7]	N.C.	N.C.	N.C.	N.C.	GND
6	GND	N.C.	TEMP_VDD_1	N.C.	N.C.	N.C.	GND
5	GND	N.C.	TEMP_DQ_1	N.C.	N.C.	N.C.	GND
4	GND	N.C.	TEMP_GND_1	N.C.	N.C.	N.C.	GND
3	GND	N.C.	TEMP_VDD_0	N.C.	N.C.	N.C.	GND
2	GND	N.C.	TEMP_DQ_0	N.C.	N.C.	N.C.	GND
1	GND	N.C.	TEMP_GND_0	N.C.	N.C.	N.C.	GND
Pin	Z	A	B	C	D	E	F

Table 5-8 ACOP-SBC J4 Pin Function

[6] TBC

[7] TBC

- P1 (Front panel connector): for software development and debugging. This connector is a Glenair M83513/04-A09N with pins numbered as in the table below:

Pin	Signal Name	Function
1	EXT-RESET*	External reset input
2	UART0-RX-	UART 0 receive data
3	UART0-TX-	UART 0 transmit data
4	UART0-RX+	UART 0 receive data
5	UART0-TX+	UART 0 transmit data
6	GND	Signal ground
7	GND	Signal ground
8	N.C.	
9	N.C.	

Table 5-9 ACOP-SBC Front Panel P1 Connector Pin Function

5.3.4 ELECTRICAL CHARACTERISTICS

o Power supply
- 3.3V +/- 5%, 3A (typ.), 3.6A (max), CPU running at 400MHz
- 3V power source from the CompactPCI backplane
- No special requirement for power-up sequence
- Power monitor circuit for both 3.3V and 5V supplies from ACOP-PS

o Electromagnetic Compatibility: per MIL-STD-461E

o Power consumption: see Table 5-30 ACOP Power Budget

5.3.5 MECHANICAL CHARACTERISTICS

o Print Circuit Board (PCB)
- 10 layer PCB : ACOP-SBC PCB is constructed with two voltage planes in the center, two internal signal layers, two ground planes, two external signal layers, and two additional ground layers for thermal management purpose.
- Conformal coating to prevent damage due to moisture and humidity

0 Form Factor
- CompactPCI 6U board size with conduction cooled feature (see Table 5-1 ACOP PCB Specifications)
- Maximum component height on the back side of the card will not exceed 0.060 inches

0 Backplane Connector:
- Harting 1721 110 2102 (Type A, with upper shield) for CompactPCI J1,J4
- Harting 1724 110 2102 (Type B, with upper shield) for CompactPCI J2,J5

o Front Panel Design
- Dimension: 245.35mm (9.65 in.) x 19.8 mm (0.8 in.)

The front panel will also have a cut-out to allow for installing the connector P1:
- Connector: Glenair M83513/04-A09N
- Matting Cable: Glenair M83513/03-A09N

0 Mass: see Table 5-2 ACOP PCB Mass Budget

5.4 ACOP-T101

The block diagram in Figure 5-8 shows the main functional blocks of the ACOP-T101 board. An ACTEL A54SX72A FPGA is used to implement the PCI agent and VGA controller function. It is compliant with the PCI 2.2 specification and provides 33MHz performance. Two SRAM chips are used as video memory and buffer between system slot and the FPGA chip.

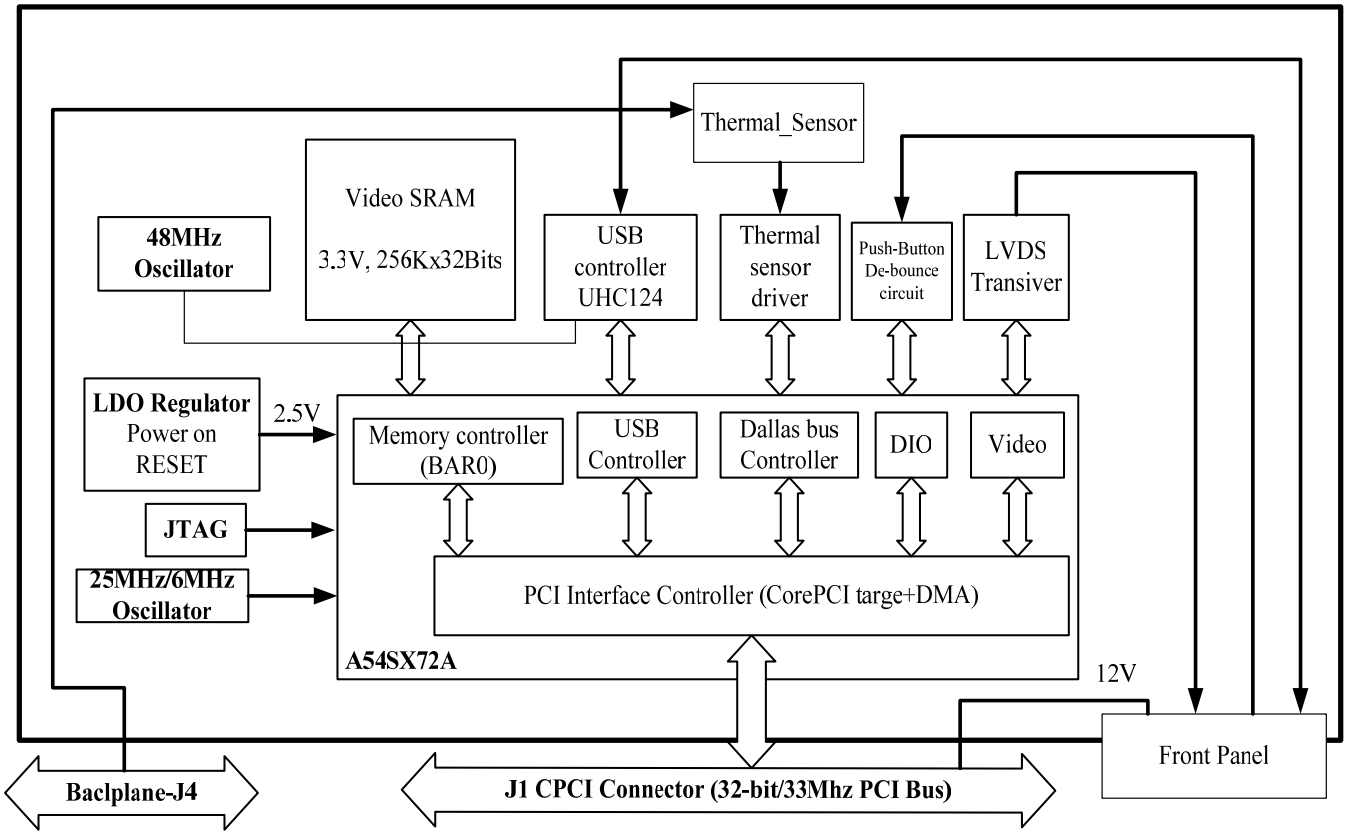

Figure 5-8 ACOP-T101 Functional Block Diagram

5.4.1 FEATURES

The following is a list of the hardware features for the ACOP-T101:

- LCD Graphic Function :
  - Only graphic mode supported.
  - Resolutions: 640x480 and 320x240
  - Color: 5 bits (bit1 to bit 5) for R, G, B. The value of bit 0 of each color is fixed to zero.
  - Clock frequency: 25MHz
  - Vertical frequency: ~ 60Hz
  - Video SRAM: 256K x 32bit
- Discrete I/O function
  - De-bounce circuit for push-button input
  - Two 1-wire buses for Dallas temperature sensor input
  - Output to adjust the brightness of the LCD backlight
- USB interface:
  - Supports USB Specification 2.0 (up to 1.5Mb/s) devices
  - Allow one PCI transaction to access both UHC124 controllers.
  - Support burst R/W by using backend throttling
- 32bits /33Mhz CompactPCI peripheral slot, PICMG 2.0 compliant

5.4.2 HARDWARE DESIGN

5.4.2.1 PCI AGENT

The PCI agent is based on Actel CorePCI 5.3.2 and implemented in the Actel FPGA A54SX72A chip with the following characteristics:

- Target function only.
- Three base addresses:
  - BAR0 (256k x 32bit) is used for the video SRAM and is mapped in the memory space.
  - BAR1 (TBC) is used for the control and status registers of LCD controller, DAC controller and SL811HS. It is mapped in the memory space.
  - BAR2 is used for the DMA control register and is mapped in the IO space.
- PCI interrupt sources are:
  - USB host controller (UHC124).
  - Four push-button inputs.

5.4.2.2 LCD CONTROLLER

The LCD controller provides control and RGB signals to the LCD pane and Implement in the Actel FPGA A54SX72A with the following characteristics:

- Mode support: Graphic mode only.
- Resolution support: 640 x 480.
- Color: 5 bit (bit1 to bit 5) for R G B. The value of bit0 of each color is fixed.
- Clock frequency: 25MHz
- Vertical frequency: ~ 60Hz
- Video SRAM: 256K x 32bit

The LCD controller also generates a PWM (pulse width modulation) signal to control the LCD brightness. The duty cycle (ON+OFF state) of the PWM signal is designed as 1600μsec. The pulse width of ON state (turn the LCD backlight ON) is set by a 4bits register. Its LSB represents 100μsec. LVDS is used as the signaling technique for all LCD signals.

5.4.2.2.1 LCD PIXEL ARRANGEMENT

The pixel arrangement of the LCD panel T-51750AA-V350 is shown in Figure 5-9.

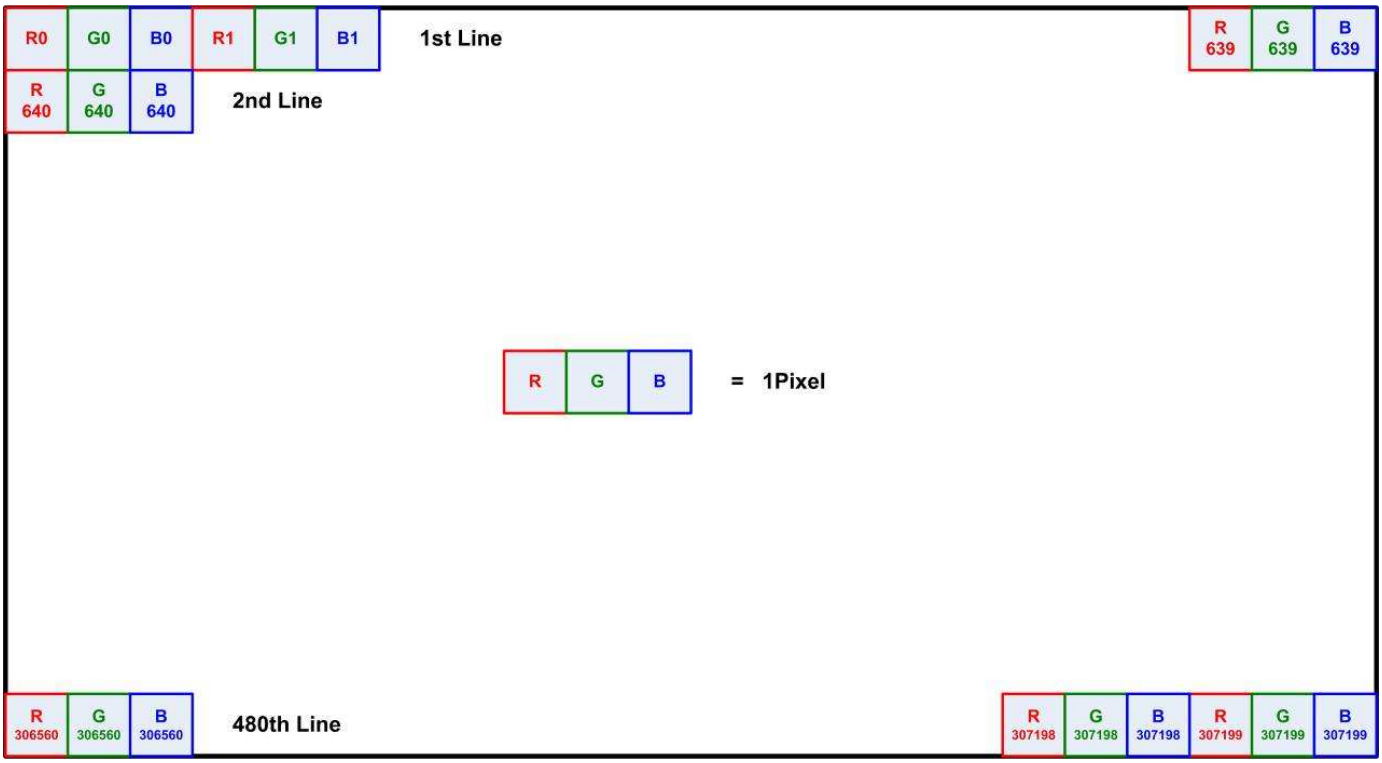

Figure 5-9 LCD pixel arrangement

5.4.2.2.2 VIDEO SRAM ARRANGEMENT

The size of SRAM to support a 640x480 screen resolution is calculated as follow:

Resolution	Bit map size with 16 bit colors	Necessary RAM on the video card
640 x 480	614,400 bytes	1 MB

Table 5-10 ACOP-T101 Video SRAM Requirement

There is 1MB SRAM installed in ACOP-T101 and used as VGA video graphics memory. The address block is defined as from Offset+0h to Offset+3ffffh.The relation between the video SRAM and the LCD pixel is shown below:

Addr/Bit	31	30~26	25~21	20~16	15	14~10	9~5	4~0
Offset+0	-	B1	G1	R1	-	B0	G0	R0
Offset+1	-	B3	G3	R3	-	B2	G2	R2
Offset+2	-	B5	G5	R5	-	B4	G4	R4
Offset+257ffh	-	B(307199)	B(307199)	R(307199)	-	B(307198)	G(307198)	R(307198)

Table 5-11 LCD Pixel to Video SRAM Map

5.4.2.3 1-WIRE BUS CIRCUIT

The 1-wire bus control circuit is designed as the master of the thermal sensor network and implemented in the Actel FPGA A54SX72A chip with the following characteristics:

- Two 1-wire (only one port pin for communication) thermal network buses to CompactPCI connector J4. Each bus includes power, data in/out and GND lines. All data and commands are transmitted LSB first over the 1-wire data in/out line.
- Provide power for each Dallas sensor.
- Capable to scan the 1-wire buses to find the device ID of Dallas sensors.
- Read the temperature value of a Dallas sensor specified by the host.

Three registers are implemented in the FPGA, one is command register for CPU to set the command of FPGA control circuit, one is pointer register provides the function to set the ID of Dallas sensors, the other is data register stores the command or data to the Dallas sensor selected by the pointer register.

5.4.2.4 USB INTERFACE

The USB function is provided by TransDimension UHC124, which supports USB 2.0 compliant full-speed and low-speed USB device. The USB to PCI interface is implemented in the Actel FPGA A54SX72A with following characters:

- Set UHC124 in a mode of the multiplexed memory access.
- Map UHC124 register and memory in PCI BAR1.
- Support single PCI R/W only.
- Bypass IRQs of UHC124 to the PCI agent.

5.4.3 EXTERNAL INTERFACES

The ACOP-T101 includes the following external interfaces:

- J1 (To ACOP Backplane): includes standard CompactPCI 32bits/32Mhz J1 signals

25	GND	5V	N.C.	N.C.	3.3V	5V	GND
24	GND	AD[1]	5V	N.C.	AD[0]	N.C.	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	N.C.	C/BE[0]#	GND
20	GND	AD[12]	GND	N.C.	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	N.C.	N.C.	GND	PERR#	GND
16	GND	DEVSEL#	GND	N.C.	STOP#	N.C.	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	KEY AREA						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	N.C.	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	Pull-up	AD[31]	GND
5	GND	N.C.	N.C.	RST#	GND	GNT#	GND
4	GND	N.C.	GND	N.C.	N.C.	N.C.	GND

3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	N.C.	5V	N.C.	N.C.	N.C.	GND
1	GND	5V	-12V	N.C.	+12V	5V	GND
Pin	Z	A	B	C	D	E	F

Table 5-12 ACOP-T101 J1 Pin Function

- J4 (To ACOP Backplane): includes peripheral input/output signals, 1 wire temperature buses

25	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
24	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
23	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
22	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
21	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
20	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
19	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
18	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
17	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
16	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
15	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
12-14	KEY AREA						
11	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
10	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
9	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND
8	GND	CHA_GND.[8]	N.C.	N.C.	N.C.	N.C.	GND
7	GND	CHA_GND.[9]	N.C.	N.C.	N.C.	N.C.	GND
6	GND	N.C.	TEMP_VDD_1	N.C.	N.C.	N.C.	GND
5	GND	N.C.	TEMP_DQ_1	N.C.	N.C.	N.C.	GND
4	GND	N.C.	TEMP_GND_1	N.C.	N.C.	N.C.	GND
3	GND	LCD 12V	TEMP_VDD_0	N.C.	N.C.	N.C.	GND
2	GND	LCD 12V	TEMP_DQ_0	N.C.	N.C.	N.C.	GND
1	GND	N.C.	TEMP_GND_0	N.C.	N.C.	N.C.	GND
Pin	Z	A	B	C	D	E	F

Table 5-13 ACOP-T101 J4 Pin Function

- P1 (To ACOP-VI): includes LCD RGB signal

Pin No.	Symbol	Function
1	REV+	
2	DENA+	Disable
3	B5+	Blue Image data (LSB)
4	B3+	Blue Image data
5	B1+	Blue Image data
6	B4+	Blue Image data
7	B2+	Blue Image data
8	B0+	Blue Image data (MSB)

[8] TBC

[9] TBC

Pin No.	Symbol	Function
9	G5+	Green Image data (LSB)
10	G3+	Green Image data
11	G1+	Green Image data
12	R4+	Red Image data
13	R2+	Red Image data
14	R0+	Red Image data (MSB)
15	VSYNC+	Vertical Synchronous signal
16	V_CLOCK+	Clock signal for sampling image digital data
17	G4+	Green Image data
18	G2+	Green Image data
19	GND	Ground
20	REV-	
21	DENA-	Disable
22	B5-	Blue Image data (LSB)
23	B3-	Blue Image data
24	B1-	Blue Image data
25	B4-	Blue Image data
26	B2-	Blue Image data
27	B0-	Blue Image data (MSB)
28	G5-	Green Image data (LSB)
29	G3-	Green Image data
30	G1-	Green Image data
31	R4-	Red Image data
32	R2-	Red Image data
33	R0-	Red Image data (MSB)
34	VSYNC-	Vertical Synchronous signal
35	V_CLOCK-	Clock signal for sampling image digital data
36	G4-	Green Image data
37	G2-	Green Image data

Table 5-14 ACOP-T101 P1 Pin Function

- P2 (To ACOP-VI): includes LCD control signal and power for LCD module

Pin No.	Symbol	Function
1	G0+	Green Image data
2	R5+	Red Image data
3	R3+	Red Image data
4	R1+	Red Image data
5	HSYNC+	Horizontal Synchronous signal Ground
6	PWM+	PWM control for backlight
7	GND	Ground

Pin No.	Symbol	Function
8	3.3V	DC 3.3V
9	3.3V	DC 3.3V
10	12V	DC12V
11	12V	DC 12V
12	12V	DC12V
13	GND	Ground
14	PUSH3	PUSH button 3
15	PUSH1	PUSH button 1
16	GND	Ground
17	G0+	Green Image data
18	R5+	Red Image data
19	R3+	Red Image data
20	R1+	Red Image data
21	HSYNC+	Horizontal Synchronous signal Ground
22	PWM+	PWM control for backlight
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	GND	Ground
29	GND	Ground
30	PUSH2	PUSH button 2
31	PUSH0	PUSH button 0

Table 5-15 ACOP-T101 P2 Pin Function

- P3: USB 0 signals
- P4: USB 1 signal
- P5: USB 2 signals
- P6 (To Locker Front Panel): USB 3 signals

The pin assignment of USB connectors is shown in the following table:

Pin	Signal Name	Function
1	VCC	5V power
2	D+	USB data
3	D-	USB data
4	GND	Ground
5	CHA GND	Chassis Ground
6	CHA GND	Chassis Ground

Table 5-16 ACOP-T101 P3/P4/P5/P6 Pin Function

5.4.4 ELECTRICAL CHARACTERISTICS

- Power supply
  - 3.3V ± 5% for LCD control circuit and Dallas sensor
  - 5V ± 5% for USB devices
  - 12V ± 5% for the LED backlight of LCD
  - No special requirement for power-up sequence
  - 3.3V, 5V and 12V power sources supplied by ACOP-BP

- Electromagnetic Compatibility: per MIL-STD-461E

- Power consumption: see Table 5-30 ACOP Power Budget

5.4.5 MECHANICAL CHARACTERISTICS

- Print Circuit Board (PCB)
  - 8 layer PCB : ACOP-T101 PCB is constructed with three voltage planes in the center, two internal signal layers, two external signal layers, and one additional ground layers for thermal management purpose
  - Conformal coating to prevent damage due to moisture and humidity

- Form Factor
  - CompactPCI 6U board size with conduction cooled feature (see Table 5-1 ACOP PCB Specifications)
  - Maximum component height on the back side of the card will not exceed 0.060 inches

- Backplane Connector:
  - Harting 1721 110 2102 (Type A, with upper shield) for CompactPCI J1,J4

- Front Panel Design
  - Dimension: 245.35mm (9.65 in.) x 19.8 mm (0.8 in.)

  Six connectors on the front panel:
  - 4 USB type A connectors
  - 2 connectors for video interface signals (1 x M83513/04-D11N and 1 x M83513/04-F11N)

- Mass: see Table 5-2 ACOP PCB Mass Budget

5.5 ACOP-T102

The ACOP-T102 board provides two transmit and one receive fiber optic interfaces meeting the ISS HRDL CCSDS packet mode standards. The interface provides intelligent reception and transmission of variable length CCSDS packets referred to in this document as frames. Frame data is received into and transmitted out of a buffer memory of 1MB contained on board. The configuration of FIFOs to manage the data is done by software allowing support for varying operational modes.

Support is provided for transmit data rate control within the interface. The software can configure a sync-symbol insertion parsing in terms of a data-symbol to sync-symbol ratio as well as specifying the number of sync-symbols between frames.

The interface removes all sync-symbols on reception.

The interface provides a means to transmit test patterns of symbols, including both valid and invalid symbols.

PCI DeviceID: 0x5309 (TBC)
PCI VendorID: 0x414D

The transmitter is capable to transmit frames from 1 to 4096 bytes length[10]. Data symbols can be interleaved with sync symbols d:s where d=0:20 s=0:20 where d is the number of consecutive data symbols and s is the number of consecutive sync symbols. Either s or d being zero means no syncs are inserted. The number of sync symbols in the gap between frames can be specified between 1 and 2 ** 23 –1 inclusively.

Receiver can receive frames from 0 to 4096 symbols with all sync symbols removed.

The hardware structure of ACOP-T102 board is shown in Figure 5-10. The PCI agent chip (Actel A54SX72A) includes the functions:

- translator between the PCI bus and interface back-end bus
- handling of the read/write operations (PCI memory space access) on the SRAM buffer
- Processing and metering data among the SRAM and TAXI physical devices

[10] The HRDL CCSDS packet size requirement is that packets will be from 100 to 4096 bytes length

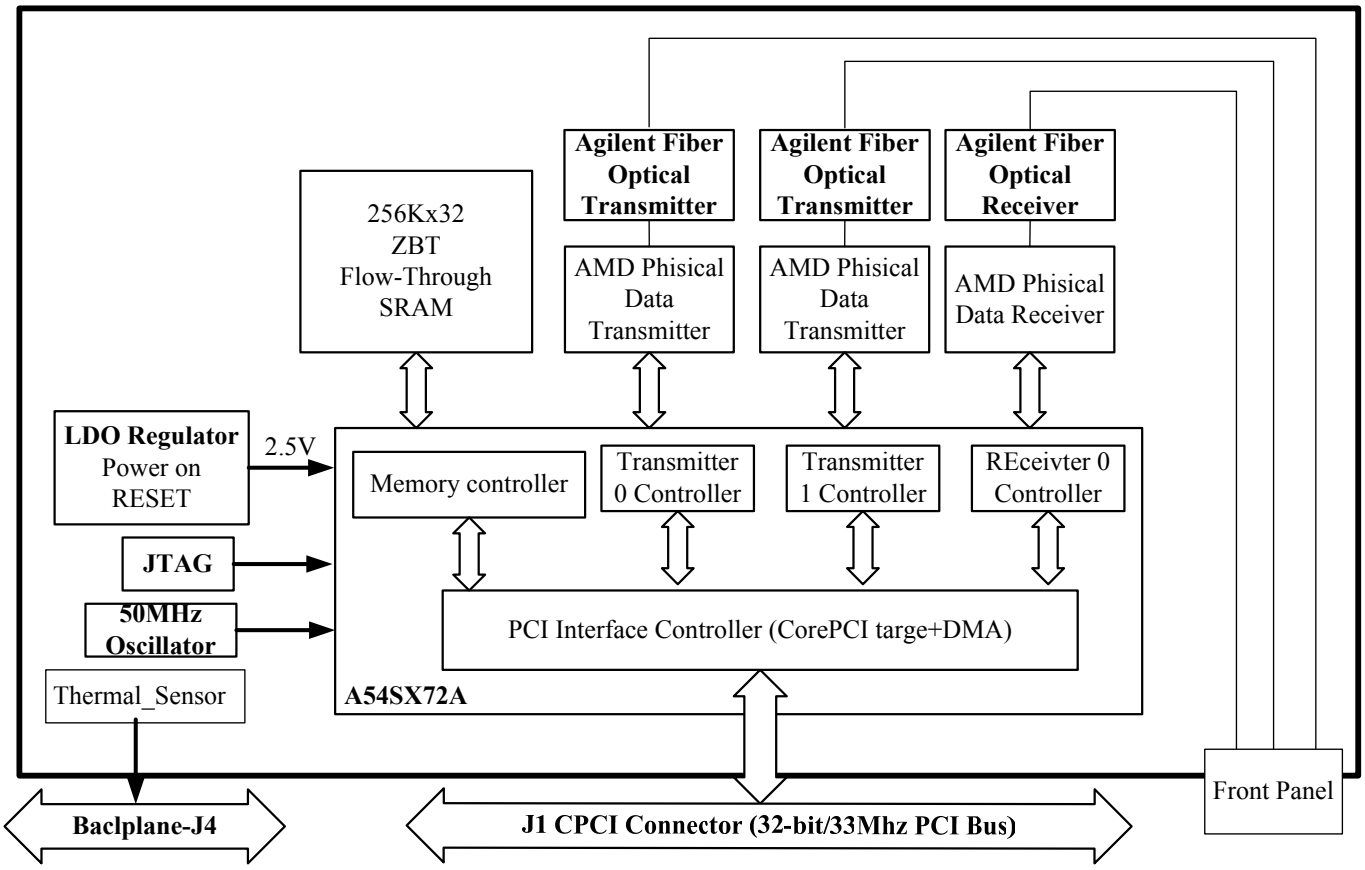

Figure 5-10 ACOP-T102 Functional Block Diagram

5.5.1 FEATURES

The following is a list of the hardware features for the ACOP-T102:

- Provides bi-directional buffering (queuing) of character data and conversion to/from TAXI serial signaling.
- Two transmit and one receive fiber optic interfaces meeting the ISS HRDL CCSDS packet mode standards
- UP to 100 Mbits/s (signaling rate is fixed to 125 Mbps) Asynchronous operation on each channel
- Provides intelligent reception and transmission of variable length CCSDS packets referred to as frames
- On board 1M bytes SRAM memory configured as FIFO like buffer for storing raw data from interface. The configuration of FIFOs to manage the data is done by software allowing support for varying operational modes.
- Software configurable sync-symbol insertion parsing in terms of a data-symbol to sync-symbol ratio as well as specifying the number of sync-symbols between frames.
- 32bits /33Mhz CompactPCI peripheral slot, PICMG 2.0 compliant

5.5.2 HARDWARE DESIGN

5.5.2.1 PCI AGENT

The PCI agent is based on Actel CorePCI 5.3.2 and implemented in the Actel FPGA A54SX72A. Signals from CompactPCI backplane are received by the PCI agent. Both target mode and DMA mode is supported for FPGA design.

5.5.2.2 PCI SPACE ORGANIZATION

ACOP-T102 uses two BAR registers as detailed below.

BAR Number	Size	Function	Mapped to
BAR0	1MB	Buffer memory for transmit and receive FIFOs.	Memory
BAR1	1MB	Control and status registers. Does not support burst transaction or byte operations. Only 8 least address bits are decoded.	Memory

Table 5-17 ACOP-T102 BAR Usage

5.5.2.3 SRAM BUFFER (BAR0)

The buffer memory is organized into three areas, each of which contains a FIFO for an interface. There are two transmit and one receive FIFO areas. The size and location of each FIFO area is determined by the software configuration of the TX0_START, TX0_END, TX1_START, TX1_END, and RX_END registers found in the BAR1 area.

Within a FIFO area the data is organized using frame descriptors.

5.5.2.4 CONTROL REGISTERS (BAR1)

BAR1 contains registers that report the status of the interface and control it's function. The register map in memory is as follows:

Name	Address		Description
TX0_STATUS	00	0	Status for transmit interface zero
TX0_CTRL	04	1	Control for transmit interface zero
TX0_GAP	08	2	Gap count for transmit interface zero
TX0_START	0C	3	Start pointer for transmit interface zero FIFO
TX0_END	10	4	End pointer for transmit interface zero FIFO
TX1_STATUS	14	5	Status for transmit interface one
TX1_CTRL	18	6	Control for transmit interface one
TX1_GAP	1C	7	Gap count for transmit interface one
TX1_START	20	8	Start pointer for transmit interface one FIFO
TX1_END	24	9	End pointer for transmit interface one FIFO
RX_STATUS	28	10	Status for receive interface
RX_CTRL	2C	11	Control for receive interface
INT_STATUS	30	12	Interrupt status

Table 5-18 ACOP-T102 BAR1 Registers

5.5.2.5 TAXI CONTROLLER

- The TAXIchip system provides a means of connecting parallel data systems over a serial link. It provides high rate data link transmission speed is up to 100 Mbits/s with actual rate set by command, signaling rate is fixed to 125 Mbps.
- AMD TAXI chips : AM79866A is used for HRDL receiver and AM79865 is for HRDL transmitter.
- HRDL communications are based on CCSDS packet

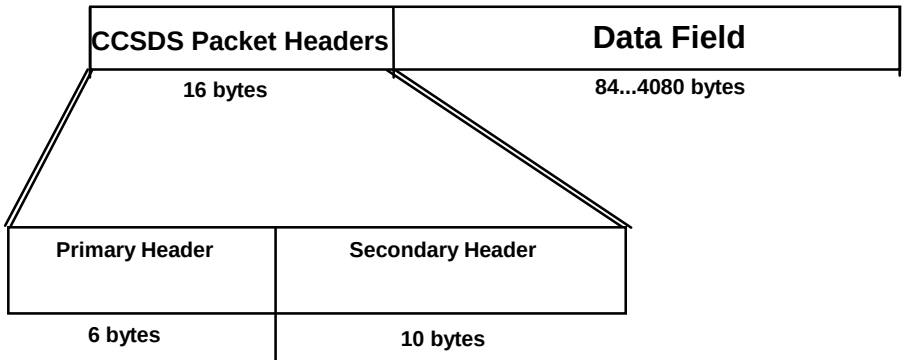

Figure 5-11 CCSDS Packet Format

- The interface controller provides intelligent reception and transmission of variable length CCSDS packets referred to as frames
- The interface controller can removes all sync-symbols on reception.
- The interface controller provides a means to transmit test patterns of symbols, including both valid and invalid symbols
- Transmitter capable to transmit frame from 1 to 4096 bytes length[11]
- Data symbols can be interleaved with sync symbols d:s where d=0:20 s=0:20 where d is the number of consecutive data symbols and s is the number of consecutive sync symbols. Either s or d being zero means no syncs are inserted
- The number of sync symbols in the gap between frames can be specified between 1 and 2 ** 23 –1 inclusively
- Receiver can receive frames from 0 to 4096 symbols with all sync symbols removed.

5.5.2.5.1 TAXI ENCODING RULE AND PROCEDURE FLOW

The protocol of HRDL communication on character layer is the TAXI rules. Each data byte or command character is encoded to two 5-bit symbols to ensure enough level transition in the serial data stream. On TX procedure, the FPGA chip should provide the 5-bit symbol flow coincident with the TAXI rules to the HRDL transmitter. On RX procedure, the output of the HRDL receiver is unframed 5-bit data. The FPGA HRDL control function will always monitor the bit stream and adjust the byte boundary at any time SYNC symbol appears. If a stable 5-bit symbol flow cannot be established, an error flags will be set in the FPGA status register.

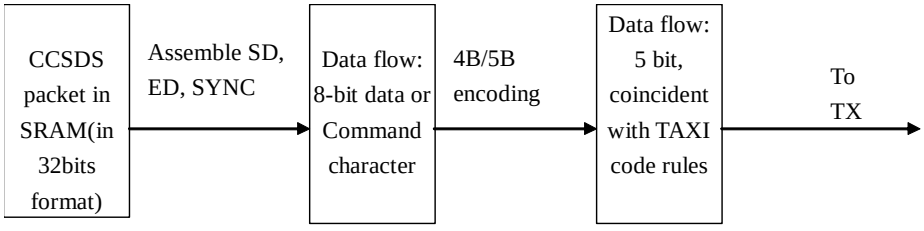

Figure 5-12 TX procedure flow

[11] The HRDL CCSDS packet size requirement is that packets will be from 100 to 4096 bytes length

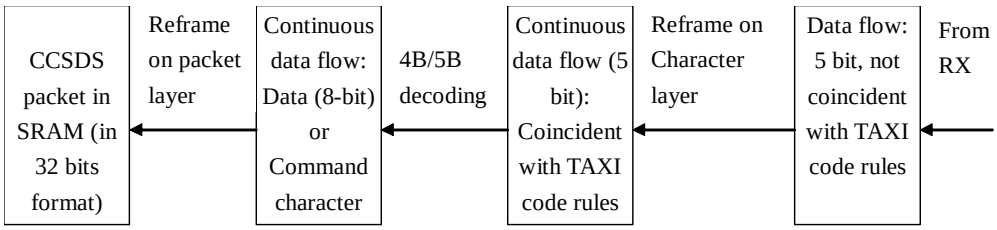

Figure 5-13 RX procedure flow

5.5.2.6 OPTICAL TRANSMITTER AND RECEIVER

The TAXI signals are concentrated and converted to/from light. The resulting optical signals are connected to the ISS APS (Automatics Payload Switch) system.

The HFBR-1116/-2116 data links are high-performance transmitter and receiver modules for serial optical data communication applications specified at 155 MBd for ATM UNI applications. These modules are designed for 50 or 62.5 mm core multimode optical fiber and operate at a nominal wavelength of 1300 nm.

The transmitter utilizes a 1300 nm surface-emitting InGaAsP LED, packaged in an optical subassembly. The LED is dc-coupled to a custom IC which converts differential-input ECL from TAXI chips into an analog LED drive current.

The receiver utilizes an InGaAs PIN photodiode coupled to a custom silicon transimpedance preamplifier IC. The PIN preamplifier combination is coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Signal Detect function. Both the Data and Signal Detect Outputs are differential ECL which compatible to TAXI chips input level.

The overall package concept for the Data Links consists of the following basic elements: two optical subassemblies, two electrical subassemblies, and the outer housings as illustrated in the following figure.

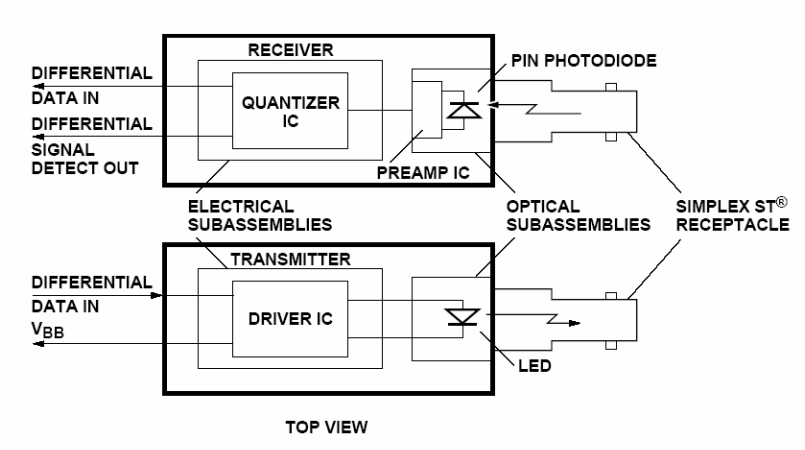

Figure 5-14 Optical Parts

5.5.3 EXTERNAL INTERFACE

The ACOP-T102 includes the following external interface:

- J1 (To ACOP-BP Backplane): includes standard CompactPCI 32bits/32Mhz J1 signals (see Table 5-12 for the pin function)
- J4 (To ACOP-BP Backplane): includes peripheral input/output signals, 1-wire temperature buses (see Table 5-13 for the pin function)
- P1 (To Locker Front Panel): Fiber optic TX 1 port
- P2 (To Locker Front Panel): Fiber optic TX 2 port
- P3 (To Locker Front Panel): Fiber optic RX1 port

5.5.4 ELECTRICAL CHARACTERISTICS

o Power supply
  - 3.3V ± 5% for FPGA control circuit and SRAM
  - 5V ± 5% for AMD TAXI chips
  - No special requirement for power-up sequence
  - 3.3V and 5V power sources supplied by ACOP-BP

o Electromagnetic Compatibility: per MIL-STD-461E

o Power consumption: see Table 5-30 ACOP Power Budget

5.5.5 MECHANICAL CHARACTERISTICS

o Print Circuit Board (PCB)
  - 8 layer PCB: ACOP-T102 PCB is constructed with two voltage planes in the center, two internal signal layers, two external signal layers, and two additional ground layers for thermal management purpose
  - Conformal coating to prevent damage due to moisture and humidity

0 Form Factor
  - CompactPCI 6U board size with conduction cooled feature (see Table 5-1 ACOP PCB Specifications)
  - Maximum component height on the back side of the card will not exceed 0.060 inches

0 Backplane Connector:
  - Harting 1721 110 2102 (Type A, with upper shield) for CompactPCI J1,J4

o Front Panel Design
  - Dimension: 245.35mm (9.65 in.) x 19.8 mm (0.8 in.)

  HRDL connectors on the front panel:
  - Fiber transmitter: Agilent HFBF-1116T
  - Fiber receiver: Agilent HFBR-2116T

0 Mass: see Table 5-2 ACOP PCB Mass Budget

5.6 ACOP-T103

The ACOP-T103 provides four (4) separate SATA channels to access storage media such as hard disk drive. It uses a PCI-to-Quad-SATA Controller that supports a 32-bit, 66 or 33MHz PCI bus. It accepts host commands through the PCI bus, processes them and transfers data between the host and Serial ATA devices.

It can be used to control four independent Serial ATA channels: each channel has its own Serial ATA bus and will support one Serial ATA device with a transfer rate of 1.5 Gbits/sec (150 MBytes/sec). An industry standard PCI-to-PCI Bridge is used to support a 32bits internal PCI path at 33 MHz, for 132 MB/s operation.

The ACOP-T103 also provides two independent high-performance Fast Ethernet interface controller ports.

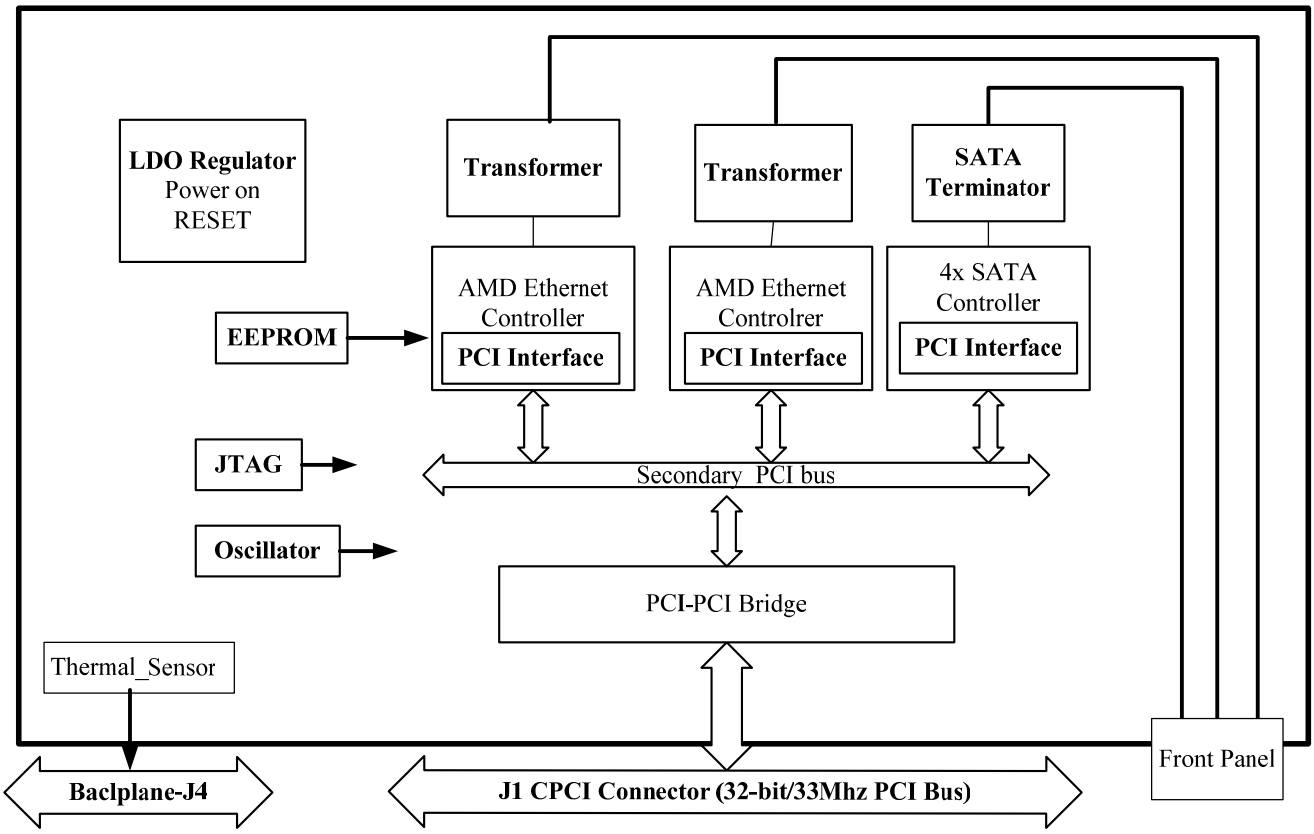

Figure 5-15 ACOP-T103 Functional Block Diagram

5.6.1 FEATURES

The following is a list of the hardware features for the ACOP-T103:

- PCI to 4-port Serial ATA (SATA) host controller
- Serial ATA transfer rate of 1.5Gbit/second
- Spread spectrum receiver and single PLL for all channels
- Independent 256 byte (32-bit by 64) FIFO per channel
- Integrated Serial ATA Link and PHY logic
- Compliant with Serial ATA 1.0 specifications
- Two IEEE802.3 10/100Base Ethernet ports, Both TX and RX supported
- 32bits /33Mhz CompactPCI peripheral slot, PICMG 2.0 compliant

5.6.2 HARDWARE DESIGN

5.6.2.1 PCI BRIDGE

The TI 2250 PCI bridge chip is used as a PCI bridge within ACOP-T103 board. It is fully complies with the *PCI Local Bus Specification*, *Revision 2.1*. It provides a connection between two independent PCI buses. The two PCI buses are referred to as the primary PCI bus, which is the PCI bus closest to the host CPU, and the secondary PCI bus, which is the PCI bus farthest from the host CPU. The 2250 implements the bus mastership control for the controller chips. A two-level round-robin arbiter selects one master from the host PCI bus.

The 2250 supports buffering of simultaneous multiple posted write and delayed transactions in both directions. The 21152 allows the two PCI buses to operate concurrently. A master and target on the same PCI bus can communicate while the other PCI bus is busy

The 2250 is a transparent 32-bit, 33 MHz device. All PCI controllers on the bus are visible to the system CPU.

The wiring of the bridge to the 2250 output pin controls the mapping of PCI slot numbers to physical slots.

5.6.2.2 SATA CONTROLLER

Silicon Image SiI 3114™ is a single-chip PCI to 4-port Serial ATA (SATA) host controller. The chip is used in ACOP-T103 for access to the ACOP HDD storage systems.

Sil 3114 is based on a 32-bit/66 MHz PCI interface and provides support for four independent Serial ATA devices, compliant with the specification of 150MB/sec transfers with CRC error-checking

The Sil 3114 includes four independent DMA channel with 256-byte FIFOs (32-bitx 64 deep) per Serial ATA channel for host reads and writes.

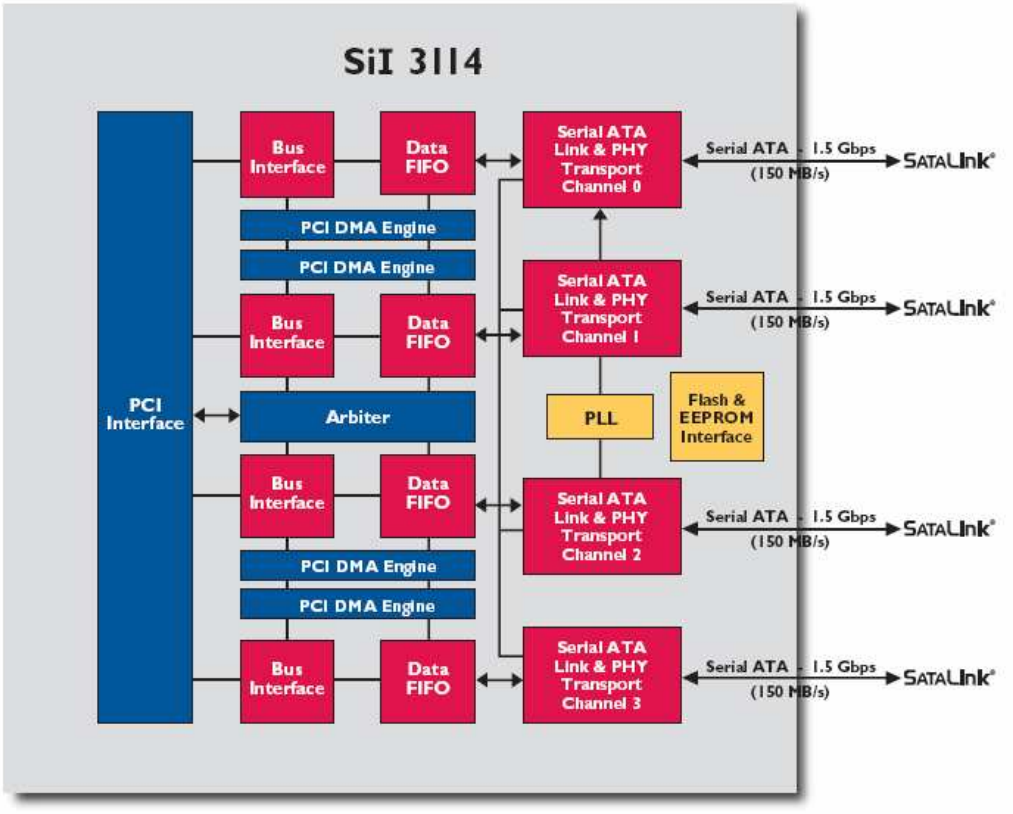

Figure 5-16 SATA Controller Organization

Four SATA data signals are wired to the SATA connectors on the board front panel:

- TX0P, TX0N, TX1P, TX1N, TX2P, TX2N, RX0P, RX0N, RX1P, RX1N, RX2P, RX2N must have a series 0.01uF capacitor.
- Layout matches the requirement for signal length and impedance matching

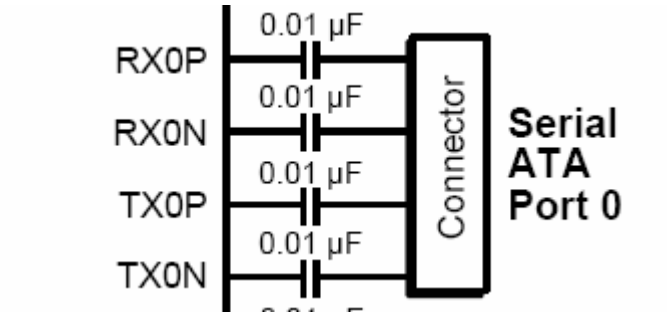

Figure 5-17 SATA Connector Signals

5.6.2.3 ETHERNET CONTROLLER

The AMD Am79C973 PCnet-FAST III chip is used as Ethernet controllers in ACOP-T103. It has a full featured physical layer device with integrated PMD sub-layers to support both 10BASE-T and 100BASE-TX Ethernet protocols. Its block diagram is shown in Figure 5-18.

The Am79C973 controllers contain 12Kbyte buffers as internal buffers which are fully programmable between the RX and TX queues for optimal performance.

The 10/100 PHY unit implements the complete physical layer for 10BASE-T and the Physical Coding Sub layer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) functionality for 100BASE-TX.

Each Ethernet connection is implemented through the single RJ-45 jack available on the board front panel, which is connected to the internal 10/100 BASE-TX transceiver of the Am79c973 chip. HALO FastJack™Ganged 10BASE-T & 10/100BASE-TX RJ-45 Connector is used to provide the Ethernet connection. The FastJack™series integrates the magnetics into an industry standard connector design.

The interface is connected directly to twisted pair media via an external 100ohm termination plus a transformer with a turns ratio of 1:1.414 (device: cable) on transmit and 1:1 on receive.

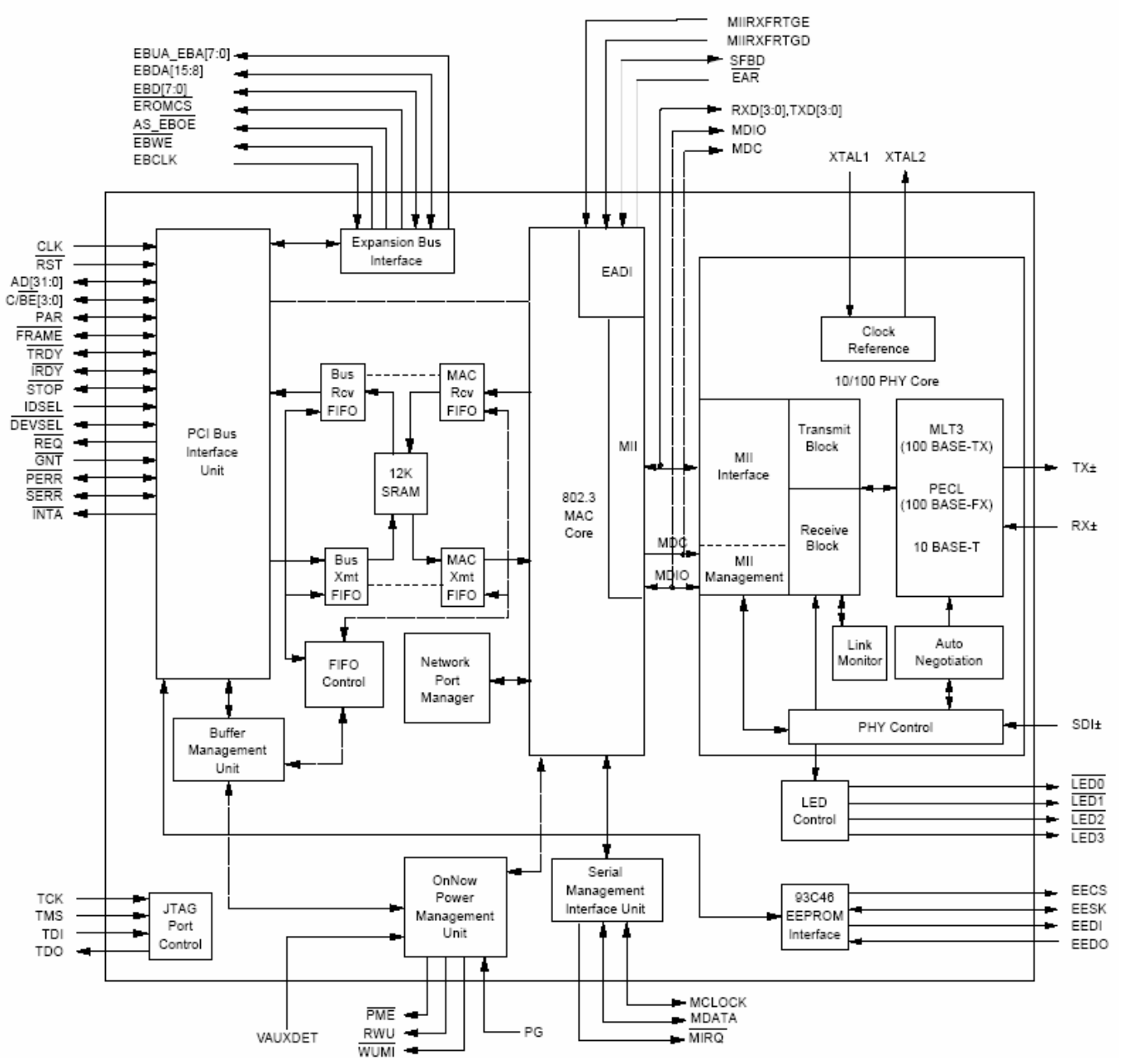

Figure 5-18 Ethernet Chip Block Diagram

5.6.3 EXTERNAL INTERFACE

The ACOP-T102 includes the following external interface:

- J1 (To ACOP Backplane): includes standard CompactPCI 32bits/32Mhz J1 signals (see Table 5-12 for the pin function)
- J4 (To ACOP Backplane): includes peripheral input/output signals, 1 wire temperature buses (see Table 5-13 for the pin function)
- P1 (To HDD1): SATA 1 Data port
- P2 (To HDD2): SATA 2 Data port
- P3 (To HDD3): SATA 3 Data port
- P4 (To HDD4): SATA 4 Data port

Pin	Signal Name	Definition	I/O
S1	GND	Ground	
S2	RX+	Differential signal from Phy	In
S3	RX-	Differential signal from Phy	In
S4	GND	Ground	
S5	TX-	Differential signal from Phy	Out
S6	TX+	Differential signal from Phy	Out
S7	GND	Ground	

Table 5-19 ACOP-T103 SATA Data Port Pin Function

- P5 (To Locker Front Panel): 10/100 Ethernet 1 port
- P6 (To Locker Front Panel): 10/100 Ethernet 2 port

Pin	Signal Name
1	TX+*
2	TX-
3	RX+
4	Not used
5	Not used
6	RX-
7	Not used
8	Not used

Table 5-20 ACOP-T103 RJ45 Ethernet Port Pin Function

5.6.4 ELECTRICAL CHARACTERISTICS

o Power supply
  - 3.3V ± 5%
  - No special requirement for power-up sequence
  - 3.3V power source supplied by ACOP-BP

o Electromagnetic Compatibility: per MIL-STD-461E

o Power consumption: see Table 5-30 ACOP Power Budget

5.6.5 MECHANICAL CHARACTERISTICS

- Print Circuit Board (PCB)
  - 8 layer PCB: ACOP-T103 PCB is constructed with two voltage planes in the center, two internal signal layers, two external signal layers, and two additional ground layers for thermal management purpose
  - Conformal coating to prevent damage due to moisture and humidity

- Form Factor
  - CompactPCI 6U board size with conduction cooled feature (see Table 5-1 ACOP PCB Specifications)
  - Maximum component height on the back side of the card will not exceed 0.060 inches

- Backplane Connector:
  - Harting 1721 110 2102 (Type A, with upper shield) for CompactPCI J1,J4

- Front Panel Design
  - Dimension: 245.35mm (9.65 in.) x 19.8 mm (0.8 in.)

  Six connectors on the front panel:
  - 2 x RJ45 Ethernet connectors
  - 4 X SATA CONNECTORS

- Mass: Table 5-2 ACOP PCB Mass Budget

5.7 ACOP-BP

The ACOP backplane is compliant with the PICMG 2.0 R3.0 standard for backplane, module connectors, mechanical and power interfaces. CompactPCI signals are routed on P1 connector row only. P2 connector is installed only on the system slot position. P3 connector row is not used at all.
Each of the CompactPCI segment provides +3.3Vdc signal environment only. All V(I/O) pins of each slot are connected to the corresponding +3.3V power planes. The peripheral interface signals for ACOP specific applications are routed on P4.

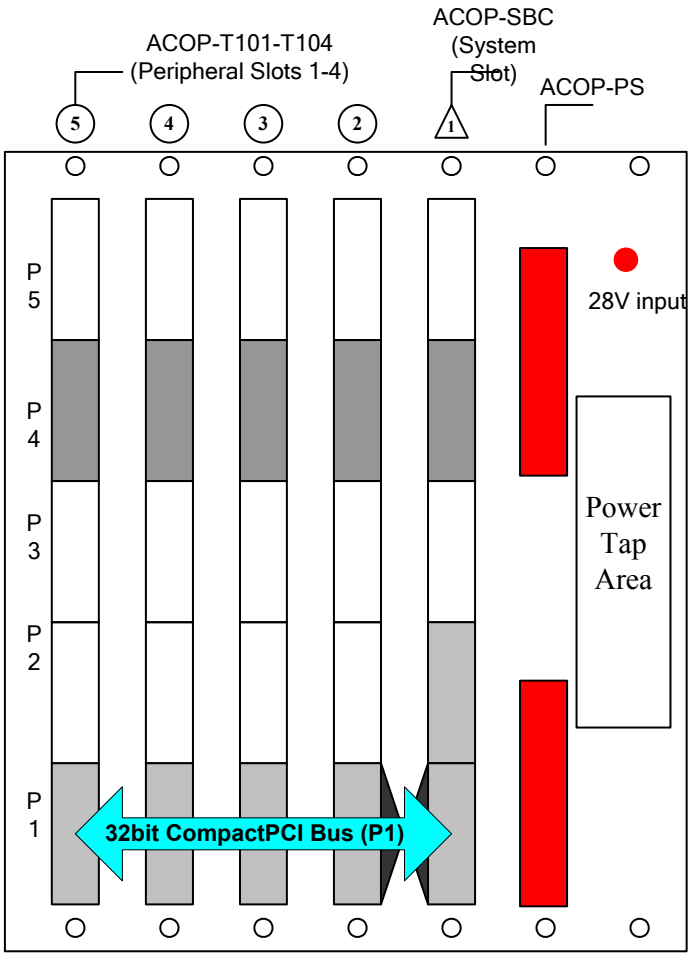

Figure 5-19 ACOP-BP Functional Block Diagram

5.7.1 FEATURES

The following is a list of the hardware features for the ACOP-BP:

- Compliant with the CompactPCI core specification (PICMG 2.0 R3.0), excluded the power for +12V and -12V power lines
- Support 32-bit, 33 MHz PCI bus operation
- 28V input to ACOP-PS
- Separate 12V distribution
- 3.3V V(I/O) signaling voltage only
- no Hot Swap capability, no Rear I/O capability
- 5-slot wide, one system and four I/O slots
- Standard 47 pins power supply slot
- Power terminals on ACOP-BP for distribution of regulated power to other ACOP devices.

5.7.2 BACKPLANE DESIGN

5.7.2.1 CHARACTERISTIC IMPEDANCE

CompactPCI signal traces meet the impedance requirement Zo = 65 Ohms ±10%

5.7.2.2 COMPACTPCI SIGNAL LAYOUT RULE

- SYSEN# grounded at system slot.
- REQ64#, ACK64#, ENUM#, FAL#, DEG#, PRST#, the JSBC Slot board shall terminate signals with 2.7KΩ pull up resistor to 3.3V
- Geographical addressing not used
- IDSEL grounded at system slots
  connected to A31 signal to ACOP-T101
  connected to A30 signal to ACOP-T102
  connected to A29 signal to ACOP-T103
  connected to A28 signal to ACOP-T104
- REQx#/GNTx# signal connections:
  REQ0#/GNT0# on system slot connected to ACOP-T101 REQ#/GNT#
  REQ1#/GNT1# on system slot connected to ACOP-T102 REQ#/GNT#
  REQ2#/GNT2# on system slot connected to ACOP-T103 REQ#/GNT#
  REQ3#/GNT3# on system slot connected to ACOP-T104 REQ#/GNT#
- CLKx signal connections (a single clock line per peripheral slot):
  CLK1 provided the clock to ACOP-T101
  CLK2 provided the clock to ACOP-T102
  CLK3 provided the clock to ACOP-T103
  CLK4 provided the clock to ACOP-T104
  Clock distribution scheme designed to accommodate up to 1.2ns (max) of skew
- INTA# -INTD# connections according the PICMG 2.0 R3.0)
- Any other CompactPCI signals in all slots within the CompactPCI segments bussed with the PICMG 2.0 R3.0 Specification.
- V(I/O) will be connected to 3.3V

5.7.2.3 POWER DISTRIBUTION

Voltage	Decoupling Capacitor	Part Number	Capacitor Rated Voltage
5V	22uF+/-10%	CWR11HH226KC	15V
	0.1uF+/-10%	1206B104K101YHT	50V
3.3V	22uF+/-10%	CWR11HH226KC	15V
	0.1uF+/-10%	1206B104K101YHT	50V

Table 5-21 Power Decoupling Components

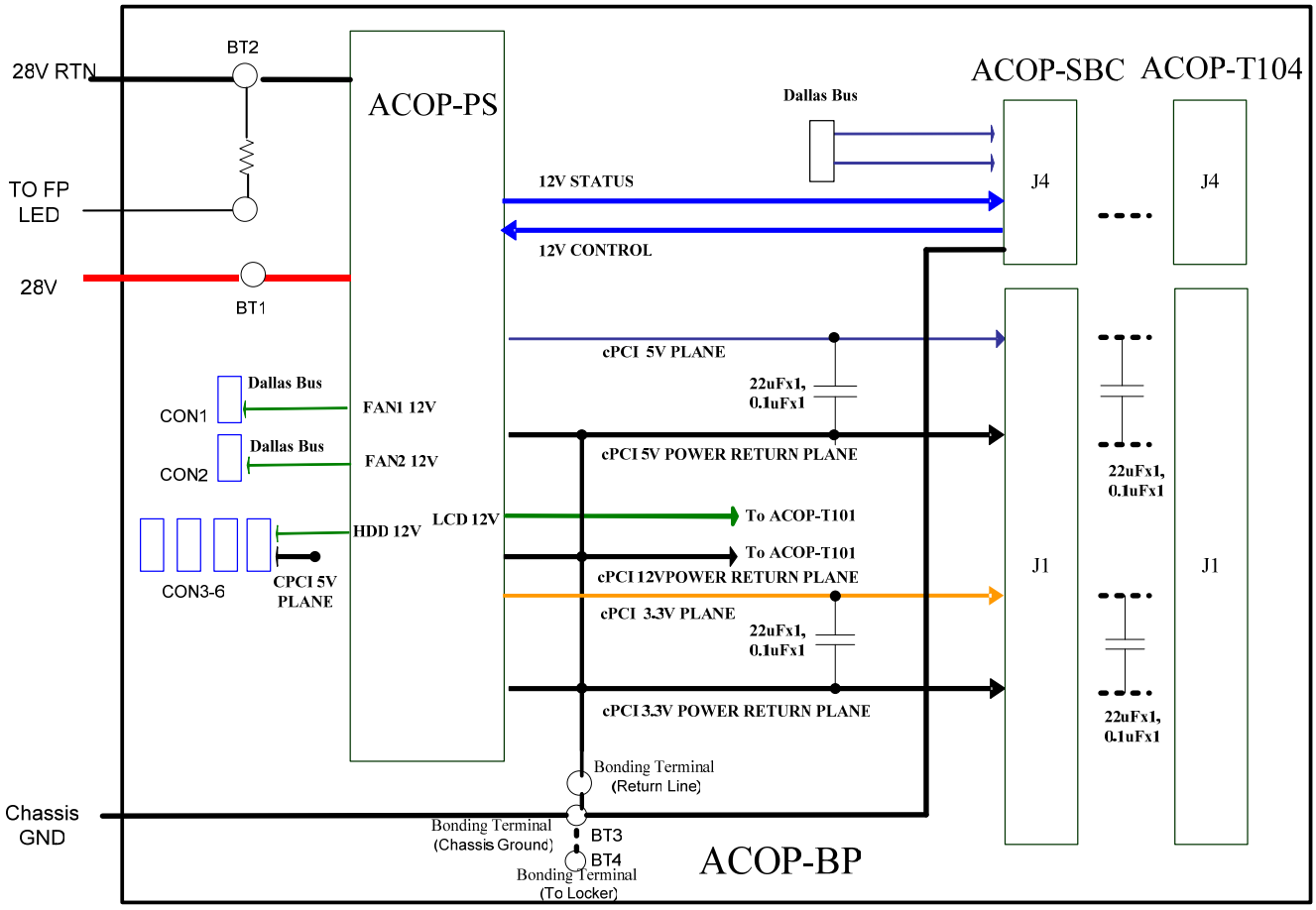

Figure 5-20 Power Distribution Block Diagram

5.7.2.4 POWER TERMINALS

The ACOP-BP includes the following power terminals for other ACOP devices:

- BT1 (From Power Switch): 28V
- BT2 (From Power Connector J1): 28V RTN
- BT3 (From Power Connector J1): Chassis GND
- BT4 (To Locker): Chassis GND
- CON1 (To Fan1): power supply and temperature monitoring
- CON2 (To Fan2): power supply and temperature monitoring

- CON3 (To HDD1): 12V and 5V
- CON4 (To HDD2): 12V and 5V
- CON5 (To HDD3): 12V and 5V
- CON6 (To HDD4): 12V and 5V

5.7.3 MECHANICAL CHARACTERISTICS

o Print Circuit Board (PCB)
- 10 layer PCB
- Conformal coating to prevent damage due to moisture and humidity

0 Form Factor
- Custom size with conduction cooled feature (see Table 5-1 ACOP PCB Specifications)

0 Backplane Connector:
- Harting 1701 154 2203 (Vertical male ,Type A, with upper shield) for CompactPCI P1, P4
- Harting 1741 154 2203 (Vertical male, Type B, with upper shield) for CompactPCI P2
- Positronic Industries PCIH47F9300A1 for ACOP-PS power supply

0 Mass: see Table 5-2 ACOP PCB Mass Budget

5.8 ACOP-PS

The ACOP-PS module is CompactPCI form factor and installed in the backplane. The input voltage range is 24 to 32Vdc, compliant with the +28Vdc power feeder voltage range provided by the EXPRESS Rack.

Three outputs (generated by power DC/DC converters implemented with hybrid integrated circuits) provide 3.3Vdc, 5Vdc and 12Vdc power supplies with independent output regulation. The outputs of the ACOP-PS adopted the power interface requirements of PICMG specification for CompactPCI systems.

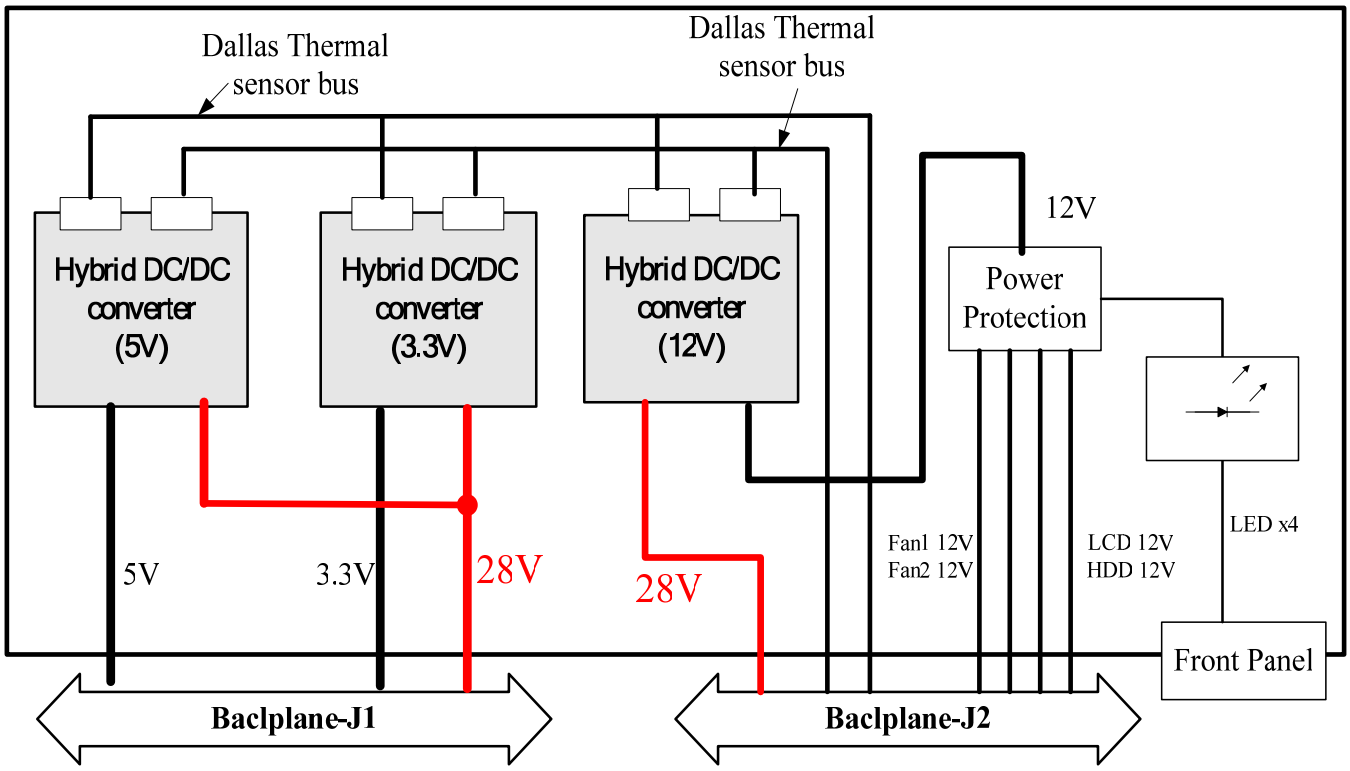

Figure 5-21 ACOP-PS Functional Block Diagram

5.8.1 FEATURES

The following is a list of the hardware features for the ACOP-PS:

- Input voltage range: 28Vdc ± 4Vdc
  (compliant with the EXPRESS Rack power specification 28Vdc +1.5Vdc / -2.5Vdc)
- Output voltages: +5.06V +/-3% ,+3.36V +/-3%,+12.1V +/-5%
- Efficiency: > 75% @ full load, nominal line
- DC/DC converters built-in protections: over-voltage, over-current, over temperature
- DC/DC converters isolation:
  Input to case: 500Vdc
  Input to output: 500Vdc
  Output to case: 100Vdc.
- DC/DC converters built-in EMI filters, meet MIL-STD-461C requirements CE01, CE03, CS01, CS02 and CS06.
- Over-current monitor and protection on 12V output lines for HDDs, LCD, Fan 1 and Fan2.
- Front panel LEDs to indicate the protection status of each 12V output line
- Backplane power connection via PICMG 2.11 compliant 47-pin power connectors.
- Environment: for Grade E MDI DC/DC converters, full output power at +125℃ (case temperature), linear derating to zero at +135℃ (case temperature).

5.8.2 SELECTION OF DC/DC CONVERTERS

According to the power budget (see Table 5-30), the load required for each power source is as following:

Voltage	3.3V	5.0V	12V
Nominal current consumption (2 HDDs are ON; 2 HDDs are in stand-by)	5.41A	2.79A	2.26A
Maximum current consumption (4 HDDs are ON, only for a short period)	5.80A	3.79A	3.68A

Table 5-22 DC/DC converters loads

ACOP-PS uses DC/DC converters from MDI, selected according to their datasheets and the ACOP power requirements. The following tables summarize the characteristics of the DC/DC converters used in ACOP and their power derating:

Part No.	5193E-S03.3F	5680E-S05F	5031SE-S12	Remarks
Input Voltage Range	18 ~ 50Vdc	18 ~ 50Vdc	18 ~ 50Vdc	At full power
Output Voltage	3.3V	5.0V	12V	
Power Rating	26.4W	30W	75W	
Current Rating	8A	6A	6.25A	
Ripple (typ)	30 mVpp	40 mVpp	60 mVpp	@2MHz bandwidth
Ripple (max)	65 mVpp	85 mVpp	150 mVpp	@2MHz bandwidth
Regulation (typ)	10 mV	10 mV	20mV	Line & Load Regulation
Regulation (max)	30 mV	50 mV	100 mV	Line & Load Regulation
Remote Sense	yes	yes	yes	

Table 5-23 MDI DC/DC converter characteristics

DC/DC Converter (Rated Voltage / Current)	5193E-S03.3F (3.3V / 8A)	5680E-S05F (5.0V / 6A)	5031SE-S12 (12V / 6.25A)
Output Power Rating	26.4W	30.0W	75W
Nominal Power Consumption Derating	17.8W 67.4%	13.9W 46.3%	27.1W 36.1%
Maximum Power Consumption Derating	19.1W 72.3%	18.9W 63.0%	44.2W 58.9%

Table 5-24 MDI DC/DC converter power derating

5.8.3 12V LOAD PROTECTION

Three types of devices in ACOP consume 12V power (HDD, LCD, Fan), they are supplied by four independent lines (HDDs, LCD, Fan 1, Fan 2). Each line is provided on the ACOP-PS with an over-current protection managed by a dedicated controller. This IC provides also the capability to shutdown each line by means of a control signal generated by the ACOP-T101 DIO interface.

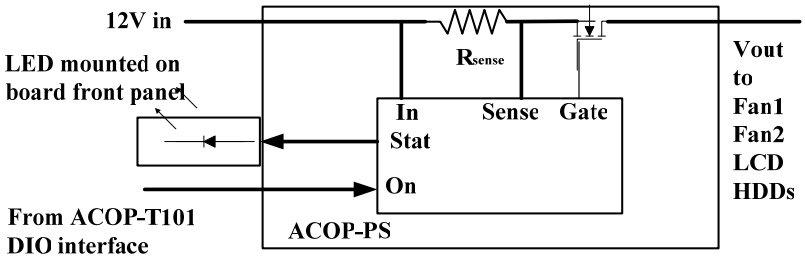

Figure 5-22 12V Load Protection Block Diagram

The controller provides startup current regulation, current glitch protection, over current protection and a status output to indicate a fault condition. Each status output drives a LED mounted on the ACOP-PS front panel.

The status output is an open-drain output which is high (LED is off) only if no fault is present. The status output goes low (LED is on) under the following conditions:

- During the UVLO (under voltage lock-out) delay period
- In startup
- When the output is forced off (On signal <0.6V)
- In an over-current condition, the threshold value is set by an external resistor
- In the retry timeout period (or latched off, for the latched parts)

5.8.4 DC/DC CONVERTERS OVER-CURRENT PROTECTION

The over-current protection within the DC/DC converters is activated between 120% and 130% of the full load rated current. There is a combination of fast current limit function (provided through a current mode circuit with pulse by pulse protection) and slow current limit function. The typical delay to switch the converter off is 5ms, and the automatic restart is after 15 to 20ms approximately.

5.8.5 DC/DC CONVERTERS OVER-VOLTAGE PROTECTION

The trip point of the over-voltage protection within the DCDC converters is typically 133% of the nominal voltage. When a control loop malfunction causes an excessive over-voltage condition, the converter will be shut-off and then automatically restarted.
The over-voltage protection circuit does not monitor the output voltage, but the output voltage as reflected to the internal auxiliary transformer winding. So, if an externally applied voltage causes the output to exceed the voltage trip limit, the converter can neither sense this over-voltage nor limit it. However, this condition is unlikely to happen in ACOP (all the voltage distribution lines are isolated and separated from each other).

5.8.6 THERMAL CONSIDERATION

Power dissipation:

The following equation is used to estimate the power dissipation:

P_{diss} = Pin – Po = Po/η– Po

where:

P_{diss}: power dissipation
Pin: power input
Po: power output
η: DC/DC converter efficiency

Po is according to Table 5-24, the efficiency is estimated according to the MDI data sheet. The following table summarizes the power dissipation calculation.

DC/DC Converter (Rated Voltage / Current / Power)	5193E-S03.3F (3.3V / 8A / 26.4W)	5680E-S05F (5.0V / 6A / 30W)	5031E-S12 (12V / 6.25A / 75W)
Nominal Power Output	17.8W	13.9W	27.1W
Maximum Power Output	19.1W	18.9W	44.2W
Estimate efficiency (from MDI data sheet)	0.65	0.71	0.77
Calculated Nominal Power Dissipation	9.6W	5.7W	8.1W
Calculated Maximum Power Dissipation	10.3W	7.7W	13.2W

Table 5-25 ACOP-PS Power Dissipation Calculation

Temperature monitoring

The temperature of each DC/DC converter is monitored by means of the 1-wire thermal sensors of the ACOP thermal monitoring network. The sensors will be mounted on the DC/DC converters cases.

Components placement and heat load to crate walls

Figure 5-23 shows the components placement on the board and the corresponding heat load conducted to the crate walls.

As shown in Figure 5-24 a heat sink under the DC/DC converters optimizes the conduction of the heat generated by power dissipation in the DC/DC converters towards the board edges and then to the crate walls. A detailed analysis is reported in the ACOP Thermal Analysis Report.

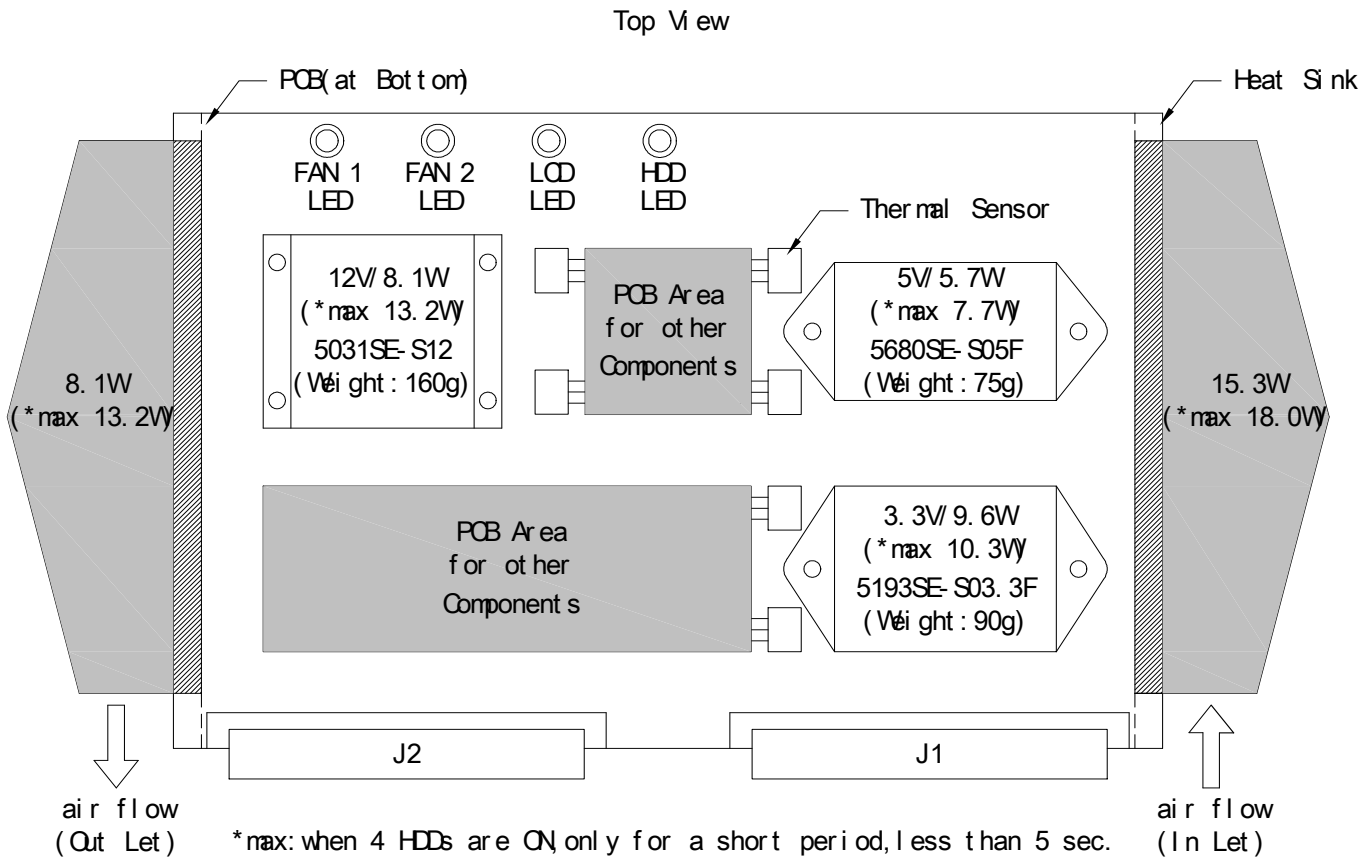

Figure 5-23 ACOP-PS components placement and heat load

5.8.7 EXTERNAL INTERFACES

The ACOP-PS includes the following external interfaces:

- J1 (To ACOP Backplane): includes standard CompactPCI power signals

Pin # (1)	Staging # (2)	Signal name	Description	Remarks
1-4	M	5.0V	5.0V Output	
5-8	M	5.0V RTN	5.0V Return	
9-13	M	3.3V RTN	3.3V Return	
14-18	M	3.3V	3.3V Output	
19-20	M	BONDING RTN	Return for Bonding	
21	M	3.3V SENSE RTN	3.3V Remote Sense Return	
22	M			N.C.
23	M			N.C.
24	M	3.3V SENSE	3.3V Remote Sense	
25	M			N.C.
26	M			N.C.
27	S			N.C.
28	M			N.C.
29	M			N.C.
30	M	5.0V SENSE RTN	5.0V Remote Sense Return	
31	M			N.C.
32	M			N.C.
33	M	5.0V SENSE	5.0V Remote Sense	
34	M			N.C.
35	M			N.C.
36	M			N.C.
37	M			N.C.
38	M			N.C.
39	M			N.C.
40	M			N.C.
41	M			N.C.
42	M			N.C.
43	M			N.C.
44	M			N.C.
45	L	CGND	Chassis Ground (safety ground)	
46	M	+DC IN	+28VDC Input	
47	M	-DC IN	+28VDC Input Return	

Note (1): pin numbers are of the female backplane connector

Note (2): L = Long length pins (first mate, last break), M = Medium length pins, S = Short length pins (last mate, first break)

Table 5-26 ACOP-PS J1 Pin Function

- J2 (To ACOP Backplane): includes 12V power distribution and control signals:

Pin # (1)	Staging # (2)	Signal name	Description	Remarks
1,2	M	FAN1/12V	FAN1/ 12VOutput	
3,4	M	FAN2/12V	FAN2/12V Output	
5,6	M	LCD/12V	LCD/12V Output	
7,8	M	12V RTN	12V Return	
9,10	M	12V RTN	12V Return	
11,12	M	12V RTN	12V Return	
13-16	M	12V RTN	12V Return	
17-20	M	HDD/12V	12V/HDD Output	
21	M	FAN1 STS	FAN1 Status	
22	M	FAN2 STS	FAN2 Status	
23	M			N.C
24	M	LCD STS	LCD Status	
25	M	HDD STS	HDD Status	
26	M			N.C.
27,28	S	CTL/STS RTN	Control and Status Return	
29	M			N.C.
30	M	FAN1 CTL	FAN1 ON/OFF Control	
31	M	FAN2 CTL	FAN2 ON/OFF Control	.
32	M			N.C.
33	M	LCD CTL	LCD ON/OFF Control	
34	M	HDD CTL	HDD ON/OFF Control	
35	M			N.C.
36	M	TSN1-1	Thermal Sensor Network 1, Pin 1	
37	M	TSN1-2	Thermal Sensor Network 1, Pin 2	
38	M	TSN1-3	Thermal Sensor Network 1, Pin 3	
39	M	TSN2-1	Thermal Sensor Network 2, Pin 1	
40	M	TSN2-2	Thermal Sensor Network 2, Pin 2	
41	M	TSN2-3	Thermal Sensor Network 2, Pin 3	
42	M			N.C.
43	M			N.C.
44	M			N.C.
45	L	CGND	Chassis Ground (safety ground)	
46	M	+DC IN	+28VDC Input	
47	M	-DC IN	+28VDC Input Return	

Note (1): pin numbers are of the female backplane connector
Note (2): L = Long length pins (first mate, last break), M = Medium length pins, S = Short length pins (last mate, first break)

Table 5-27 ACOP-BP J2 Signals

5.8.8 MECHANICAL CHARACTERISTICS

o Print Circuit Board (PCB)

- CompactPCI 6U board size with conduction cooled feature (see Table 5-1 ACOP PCB Specifications)
- Conformal coating to prevent damage due to moisture and humidity
- Heat sink used as main board, the PCB is attached to the heat sink (see figure below). This design reduces the thermal resistance between components and crate wall.

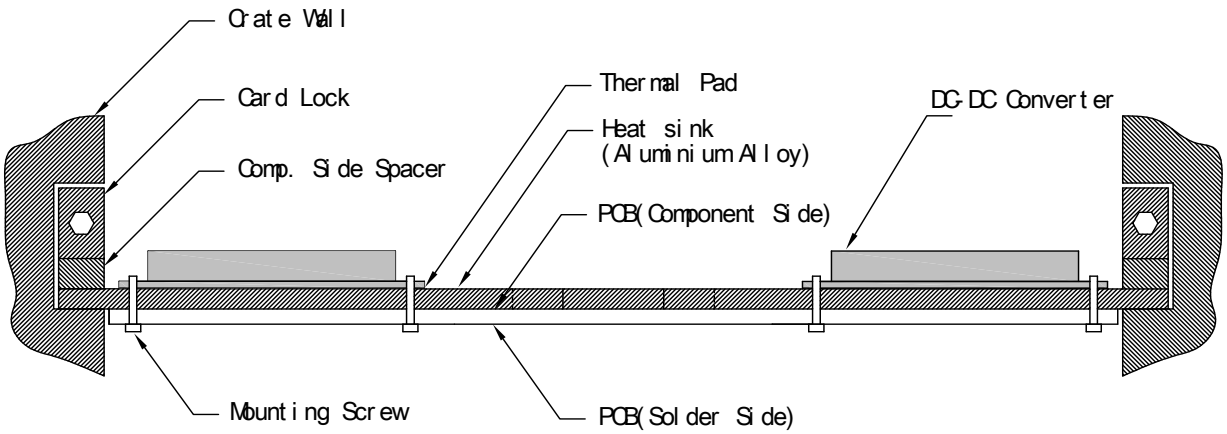

Figure 5-24 ACOP-PS Cross Section

0 Backplane Connector:

- Positronic Industries PCIH47M400A1F for backplane connectors J1, J2

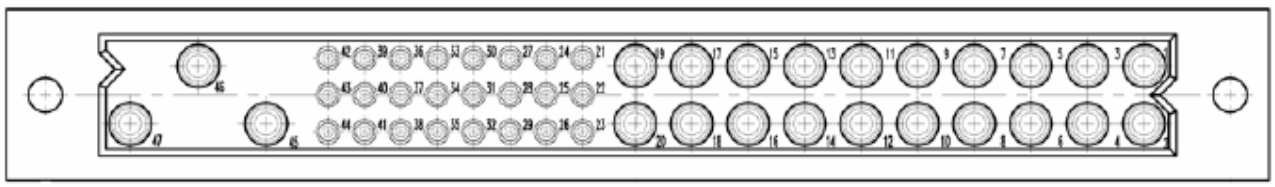

Figure 5-25 ACOP-PS Power Connector

o Front Panel Design

- Dimension: 245.35mm (9.65 in.) x 19.8 mm (0.8 in.)

Four LED visible from the front panel, showing the status of the 12V power lines for HDDs, LCD and fans:

- LED 1: status of 12V line to Fan1
- LED 2: status of 12V line to Fan2
- LED 3: status of 12V line to LCD
- LED 4: status of 12V line to HDDs

0 Mass: see Table 5-2 ACOP PCB Mass Budget

5.9 LCD MONITOR AND ACOP-VI

A Color Active Matrix Liquid Crystal Display (LCD) T-51750AA-V350 from Apollo Display with an integral LED backlight system will be mounted on the ACOP door. This TFT-LCD has a 6.5 inch diagonally measured active display area with VGA resolution (640 vertical by 480 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes.

ACOP-VI is an interface board between LCD panel and ACOP-T101, mounted on the LCD frame. It is a 4 layer PCB with the same size as the LCD frame (158mm x 120.36mm, TBC). It buffers all signals from ACOP-T101 and provides a switch circuit for the LED backlight power and dimming control. A simple switch circuit based on a power MosFET is used to switch on/off and dim the LED backlight. The PWM signal for dimming is generated from ACOP-T101. Backlight power is adjustable by means of push buttons and software.

In addition, ACOP-VI also reroutes four push-button signals to ACOP-T101.

The connections between ACOP-VI and ACOP-T101 are shown in Figure 5-26. Signal and power lines are connected through two MicroD connectors with twisted flying wires (< 18 inches):

- M83513/03-F11N (37pin) for LCD RGB signals.
- M83513/03-D11N (25pin) for LCD control signals, 3.3V and 12V.:

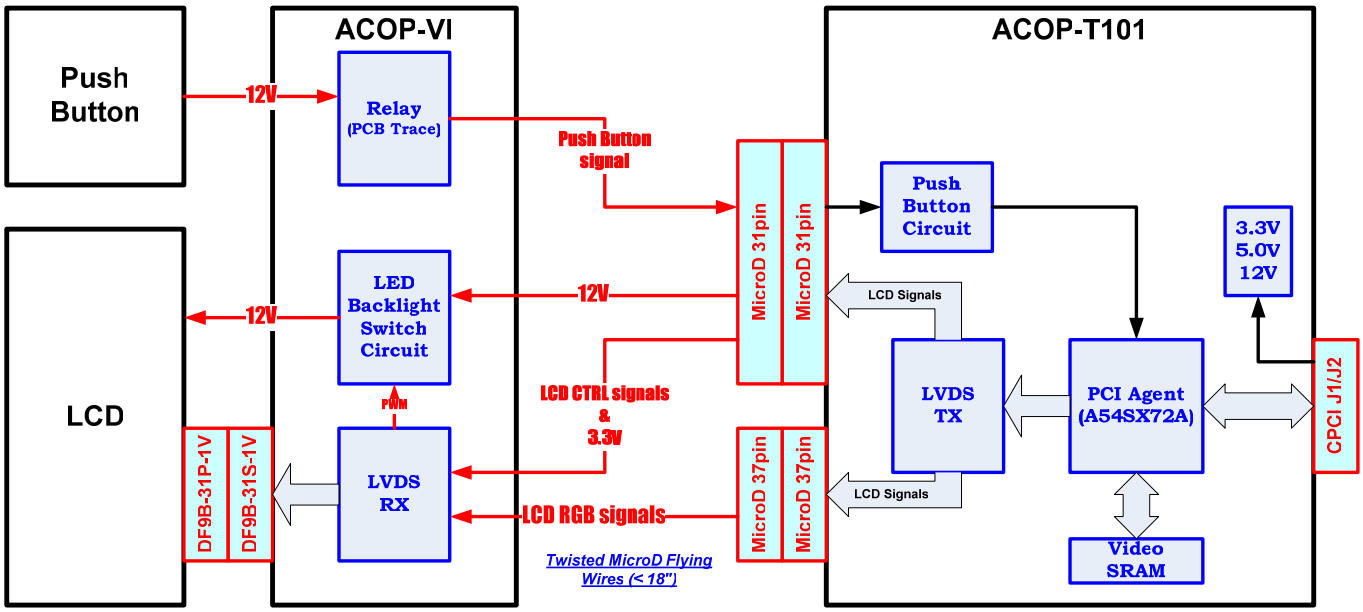

Figure 5-26 ACOP-VI to ACOP-T101 Interface

The following is a list of the hardware features for the LCD / ACOP-VI assembly:

- Compatible with VGA-480, VGA-400, VGA-350 and free format
- Screen size 6.5”
- Display format 640 x R,G,B x 480
- Display colors: 262,144 (6bits per color)
- Active area/Outline area = 62.3%
- LED backlight (two rails)
- Backlight brightness adjustable
- Power requirements: 3.3V with 180mA (typ)
  12V with 400mA (max) for the LED backlight

5.10 HARD DRIVES

The four hard drives installed in ACOP will require periodic replacement by the ISS crew from the onboard stock of empty drives. A dedicated mechanical structure in the chassis backside provides blind mate connectors for the hard drives. Cables are provided to bring power and data connections to these connectors from ACOP-T103 and ACOP-BP.

The following is a list of the hardware features for the Hard Disk Drives:

- Serial ATA with 1.5Gb/sec interface speed
- Native Command Queuing
- Build-in 16MB cache buffer
- Capacity: 200 GB or more

5.11 THERMAL SENSORS NETWORK

Thermal monitoring of ACOP will be performed by means of two thermal sensors network. Each network consists of Dallas DS18S20 one-wire bus devices attached to a single bus. Each device has a unique 64-bit serial code stored in an on-chip ROM. which allows multiple DS18S20s to function on the same one-wire bus; thus, it is simple to use one CPU to control many DS18S20s distributed over a system. The digital I/O (DIO) interface in ACOP-T101 will allow ACOP-SBC CPU to access and control the thermal network.

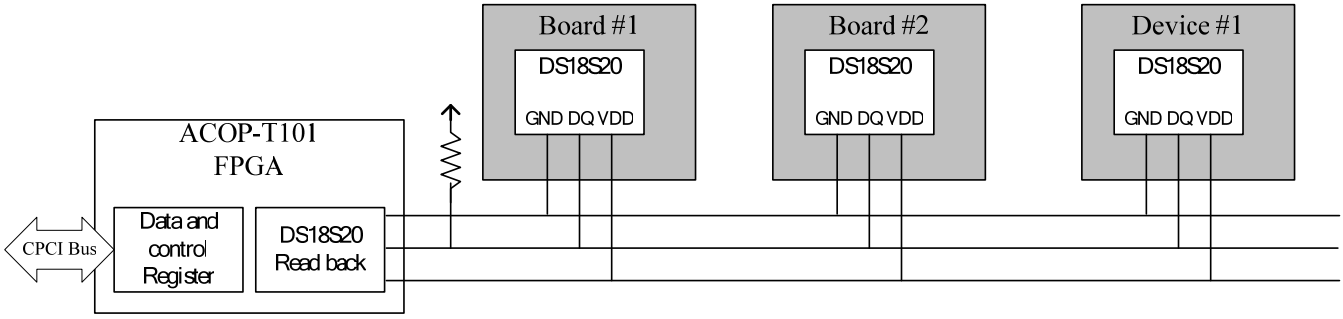

Figure 5-27 Thermal Sensor Network Block Diagram

After system power up, the Dallas sensor network operation sequence is the following::

- CPU set search command in ACOP-T101 command register to scan network for new attached sensors and store newly found Device ID (see also Figure 5-28):

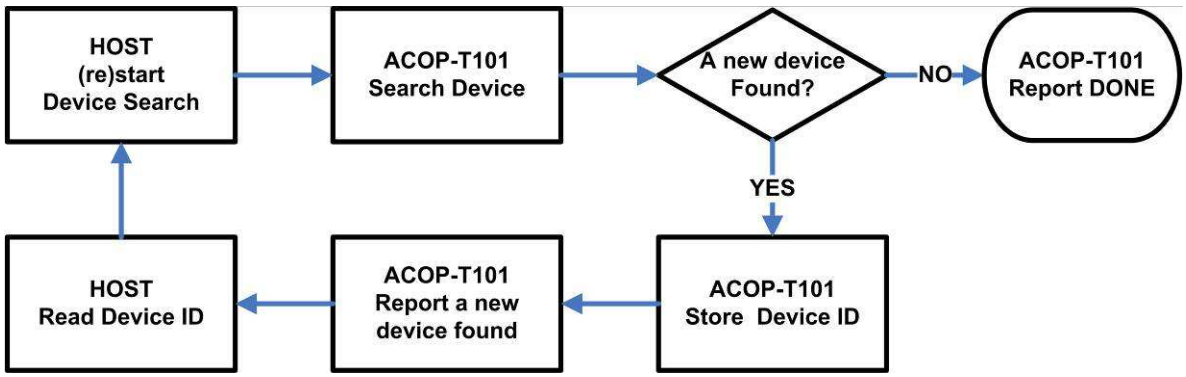

Figure 5-28 Thermal Sensors Handling

- Read and send out measured value for selected sensor.
- Read all available sensors in cycle with defined time interval; store all measured values in RAM.

The temperature sensors will be mounted where appropriate within the ACOP system (see Table 5-28 for preliminary sensor location).
For each board, the J4 backplane connector has 6 pins reserved to connect the two thermal sensors networks (three pins for each bus). Additionally, several sensors will be mounted on the chassis to monitor base plate and hard drive temperatures.
Since the Dallas sensor network is based on a flexible architecture, number and location of sensors can be easily changed to fit the ACOP needs.

Location	Item	J4 Connector Pins	Thermal Sensors Network 1	Thermal Sensors Network 2	Location
Chassis Slot PS	ACOP-PS	J4 pin 1-3	X		On 5V DC/DC Conv.
		J4 pin 4-6		X	On 5V DC/DC Conv.
		J4 pin 1-3	X		On 3.3V DC/DC Conv.
		J4 pin 4-6		X	On 3.3V DC/DC Conv.
		J4 pin 1-3	X		On 12V DC/DC Conv.
		J4 pin 4-6		X	On 12V DC/DC Conv.
Chassis Slot 1	ACOP-SBC	J4 pin 1-3	X		Board TRP
		J4 pin 4-6		X	Board TRP
Chassis Slot 2	ACOP-101	J4 pin 1-3	X		Board TRP
		J4 pin 4-6		X	Board TRP
Chassis Slot 3	ACOP-102	J4 pin 1-3	X		Board TRP
		J4 pin 4-6		X	Board TRP
Chassis Slot 4	ACOP-103	J4 pin 1-3	X		Board TRP
		J4 pin 4-6		X	Board TRP
Chassis Slot 5	ACOP-104	J4 pin 1-3	X		Board TRP
		J4 pin 4-6		X	Board TRP
HDD	HDD1		X		Plate center
				X	Plate center
HDD	HDD2		X		Plate center
				X	Plate center
HDD	HDD3		X		Plate center
				X	Plate center
HDD	HDD4		X		Plate center
				X	Plate center
Front Door	ACOP-VI		X		Board TRP
				X	Board TRP
Air Inlet	Fan		X		Near fan motor
				X	Near fan motor
Air Outlet	Fan		X		Near fan motor
				X	Near fan motor

Table 5-28 Thermal Sensors Location (TBC)

5.12 FAN CONTROL

ACOP is cooled using the Avionics Air Assembly (AAA) interface. Two fans near the inlet and outlet ports in the ACOP back plate provide the necessary airflow.

Fans are supplied by the ACOP-PS with two independent power lines provided with over-current protection and switching capability (see Para. 5.8.3). The operations of the fans will be managed to reduce acoustic noise and avoid excessive air flow, thus avoiding air recirculation.

The baseline is to turn-on one fan at a time, thus reducing noise. Since the switching capability of the ACOP-PS is controlled by the ACOP-SBC CPU, it will be possible to turn-on/off the fans according to the operative needs of ACOP.

5.13 INTERNAL HARNESS

Table 5-29 provides a list of the internal harness of ACOP. The following figures show the wiring diagrams between the parts of ACOP.

Cable	Type /Size	From	To
Ethernet x 2	CAT5 22 AWG	ACOP-T103 Card Front Panel	ACOP Front Panel (MRDL connectors)
Fiber Tx1	ISS fiber	ACOP-T102 Card Front Panel	ACOP Front Panel (HRDL connector)
Fiber Tx2	ISS fiber	ACOP-T102 Card Front Panel	ACOP Front Panel (HRDL connector)
Fiber Rx	ISS fiber	ACOP-T102 Card Front Panel	ACOP Front Panel (HRDL connector)
External Power	12 AWG	ACOP Front Panel (Power connector)	ACOP Front Panel (Circuit Breaker)
External Power	16 AWG	ACOP Front Panel (Circuit Breaker)	ACOP Front Panel (On/OFF Switch)
External Power	16 AWG	ACOP Front Panel (On/OFF Switch)	ACOP-BP
External Power Return	12 AWG	ACOP Front Panel (Power connector)	ACOP-BP
Grounding	12 AWG	ACOP Front Panel (Power connector)	ACOP-BP
LED	22 AWG	ACOP Front Panel (On/OFF Switch)	ACOP Front Panel (LED)
LED	22 AWG	ACOP Front Panel (LED)	ACOP-BP
Push Buttons	26 AWG	ACOP Door	ACOP-VI Card
LCD Ribbon Cable x 2	26 AWG	ACOP-T101 Card Front Panel	ACOP-VI Card
LCD Backlight	26 AWG	ACOP-VI Card	ACOP-LCD
USB	USB 26-28 AWG	ACOP-T101 Card Front Panel	ACOP Front Panel (USB connector)
HDD Power	24 AWG	ACOP-BP	HDD Blind Mate Connector
HDD Data	SATA 26-28 AWG	ACOP-T103 Card Front Panel	HDD Blind Mate Connector
Fans Power	26 AWG	ACOP-BP	Fans

Table 5-29 ACOP Internal Harness

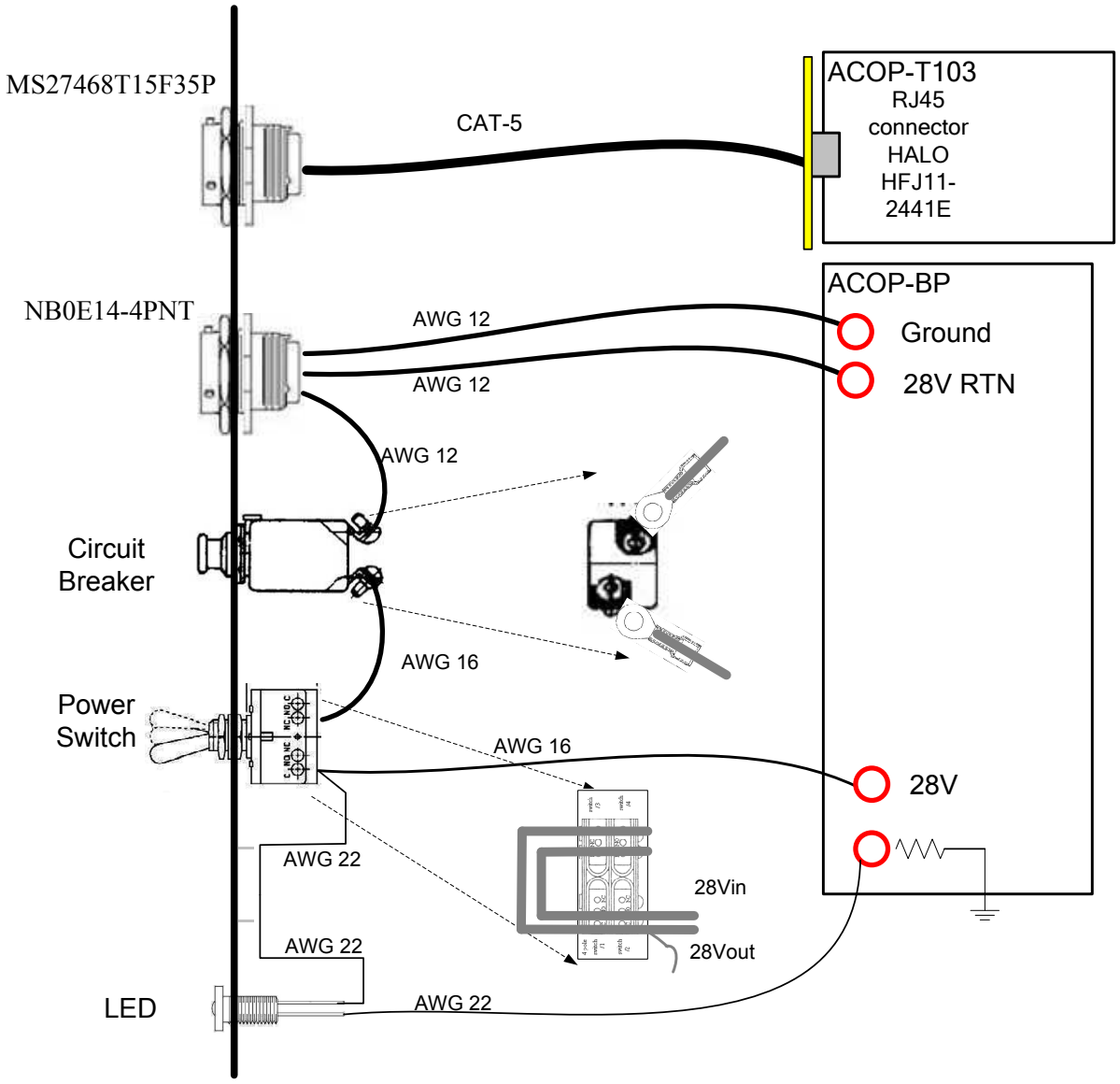

Figure 5-29 ACOP Front Panel Wiring Diagram (right side)

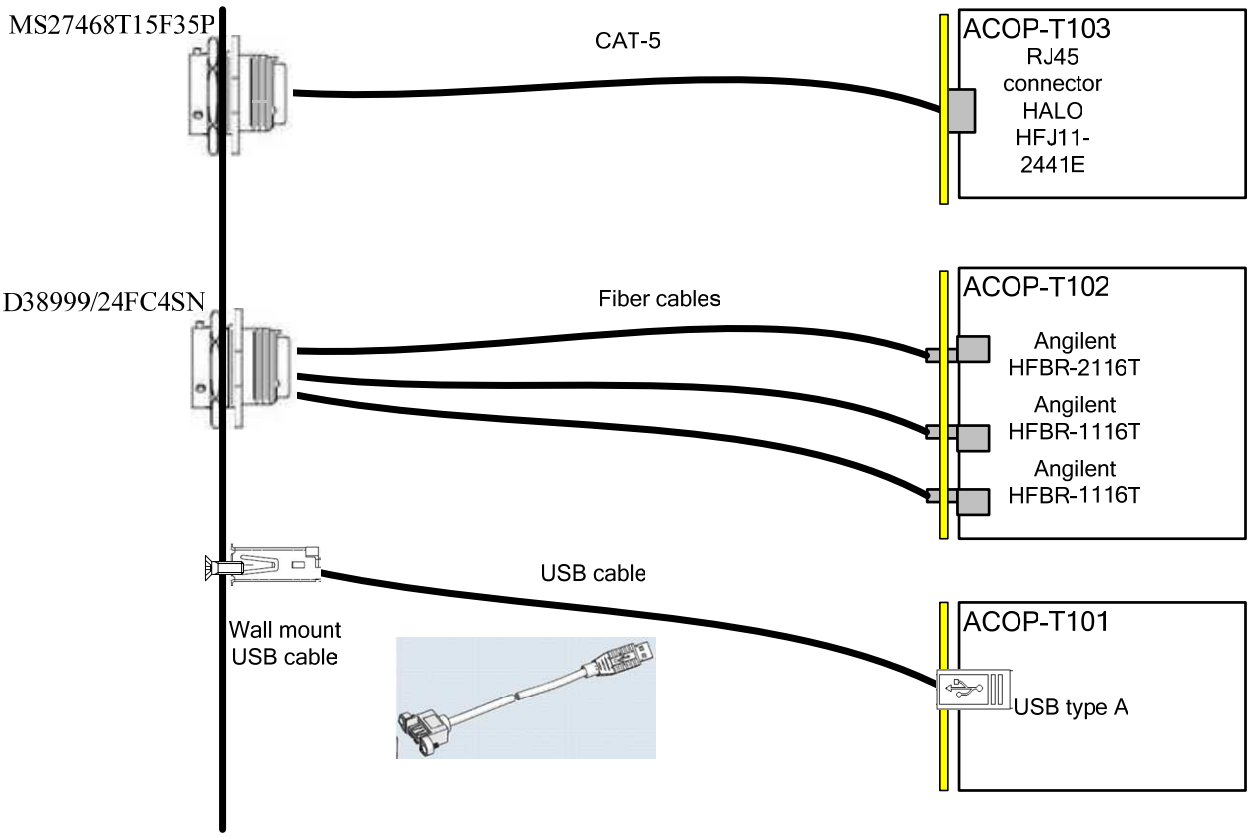

Figure 5-30 ACOP Front Panel Wiring Diagram (left side)

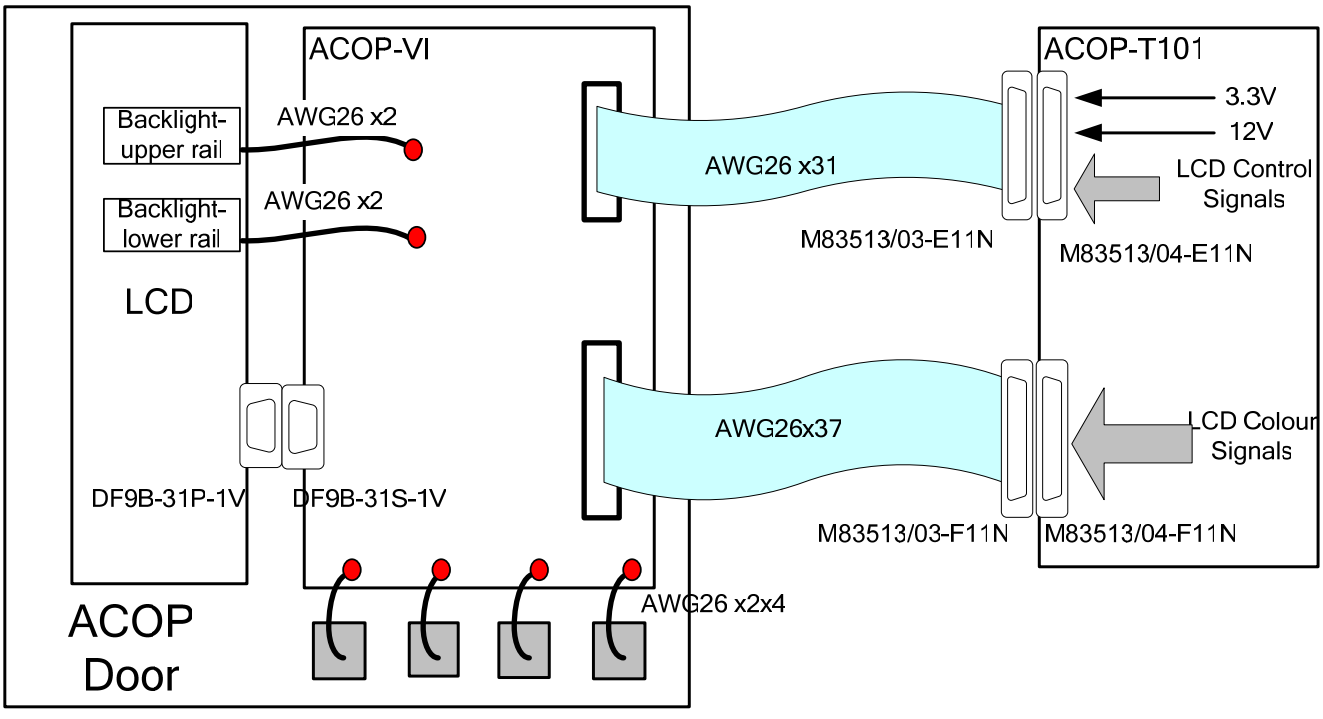

Figure 5-31 ACOP Front Panel Wiring Diagram (door)

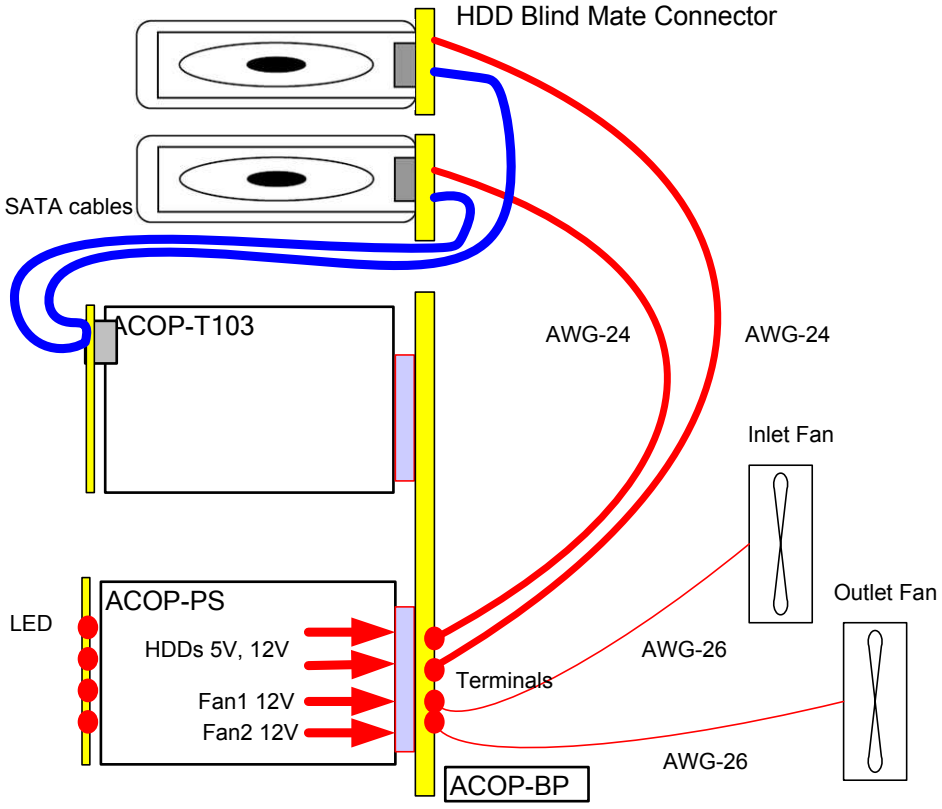

Figure 5-32 ACOP Backside Wiring Diagram (HDDs and fans, only two HDDs shown)

5.14 AVIONICS INTERFACES

This Section gives only a general overview of the ACOP Avionics Interfaces. Details are reported in the ACOP ICD.

5.14.1 POWER INTERFACES

- The power requirement will be compliant to AD1 Section 6 (Electrical Power Interfaces).
- ACOP will not be powered during STS transportation.
- On ISS, ACOP will be powered from the ER upper or lower connector panel. A cable, with connectors meeting AD1 Section 6.6 (Electrical Connectors) and Section 8 (Electrical Wiring Interface), will be provided to link ACOP's front panel power connector to the ER connector panel.
- ACOP power request is < 200Watt[12].
- ACOP input power line will be isolated from the structure by at least 1 Mohm with a parallel capacitance of <= 10uF, measured at the ACOP interface connector contacts, according to AD1 Section 7.6 (Power Circuit Isolation and Grounding)[13].
- 24Vdc to 32Vdc (nominal 28Vdc) input voltage from the power cable
- Circuit Breaker (with over-current protection and reset button) and On/Off Switch inserted in series between the ACOP power connector and the ACOP-PS.

5.14.2 DATA AND COMMANDS INTERFACES

- The Ethernet interface will meet the requirements of AD1 Section 7.7 (Signal Isolation and Grounding Requirements) and Section 9.2 (Ethernet Communications). It will provide EXPRESS rack protocol to communicate to the RIC
- A RS-422 serial interface will be available on the ACOP-SBC Card Front Panel for ground tests
- Four USB 2.0 interfaces will be available on the ACOP-T101 Card Front Panel, one of them will be connected to ACOP Front Panel to be used by crew in non-nominal scenarios (SW patches) to connect portable devices (USB keys).
- The HRDL Interfaces will meet the requirements of AD9 Section 3 and AD10 Section 3.4:
    - HRDL connections are a special resource required for ACOP that usually are not available for a standard EXPRESS Rack payload.
    - Full time – (1) TX and (1) RX fiber are used for a AMS-02 to ACOP private payload network to support the complex data management required.
    - Intermittent – (1) TX fiber is used to downlink AMS-02 telemetry data.
    - To connect the HRDL channels, optical fiber cables will be installed inside the US laboratory from ACOP to two J7 connectors on UIP panel, following a defined path agreed between EPIM and AMS-02 Program.

[12] See Section 5.15 for the actual power budget

[13] For details see Section 7.1 and Section 8

5.14.3 CREW INTERFACES

- LCD
- Four momentary Push Buttons
- Aircraft style push button Circuit Breaker
- On/Off toggle Power Switch
- LED monitoring power supply presence (Power LED)

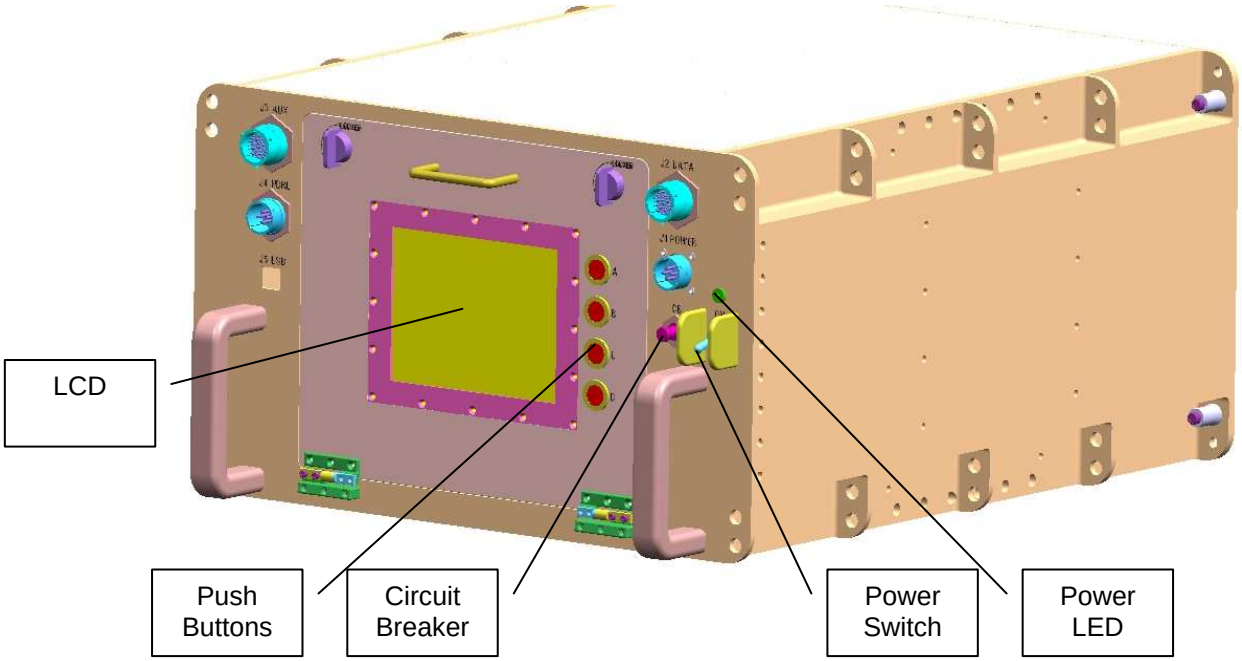

Figure 5-33 ACOP Crew Interfaces

5.15 POWER BUDGET

ACOP will have the following principal operating modes:

- Powered off
- Cold start
- Warm start
- Active idle
- Active recording
- Active playback
- Active recording and playback

The following table shows the power budget for the major components of ACOP.

LOC	Part Number	State	Type	Description	Current (mA) nom			Power (W) nom			Power (W) min	Power (W) nom	Power (W) max
					3.3V	5V	12V	3.3V	5V	12V			
CompactPCI chassis													
SLOT1	ACOP-SBC	on	Elec.	Single Board Computer	2605	0	0	8,60	0,00	0,00	8,6	8,60	9,9
SLOT2	ACOP-T101	on	Elec.	CompactPCI 6U USB and Video	500	0	0	1,65	0,00	0,00	1,65	1,65	1,65
SLOT3	ACOP-T102	on	Elec.	CompactPCI 6U HRDL	300	805	0	0,99	4,03	0,00	5,02	5,02	5,02
SLOT4	ACOP-T103	on	Elec.	CompactPCI 6U SATA and Ethernet	500	0	0	1,65	0,00	0,00	1,65	1,65	1,65
SLOT5	ACOP-T104	on	Elec.	Spare	1500	0	0	4,95	0,00	0,00	0	4,95	4,95
Backplane	ACOP-BP	passive	Elec.	CompactPCI Backplane	0	0	0	0,00	0,00	0,00	0	0,00	0
Fan modules													
Inlet	FAN-1	on	Elec.	Fan	0	0	140	0,00	0,00	1,68	0,90	1,68	1,68
outlet	FAN-2	on	Elec.	Fan	0	0	140	0,00	0,00	1,68	0,90	1,68	1,68
Door													
	ACOP-LCD	on	Elec.	LCD Monitor	0	160	0	0,00	0,80	0,00	0,00	0,80	0,80
	ACOP-BKL	on	Elec.	LCD Backlight	0	0	400	0,00	0,00	4,80	2,40	4,80	4,80
	ACOP-VI	on	Elec.	Video Interface	0	20	0	0,00	0,10	0,00	0,10	0,10	0,10
HDD													
HDD LOC 1	TBD	on	Elec.	Hot Plug SATA 250G HDD	0	700	750	0,00	3,50	9,00	1,48	12,50	12,50
HDD LOC 2	TBD	on	Elec.		0	700	750	0,00	3,50	9,00	1,48	12,50	12,50
HDD LOC 3	TBD	stdby	Elec.		0	200	40	0,00	1,00	0,48	0,00	1,48	12,50
HDD LOC 4	TBD	stdby	Elec.		0	200	40	0,00	1,00	0,48	0,00	1,48	12,50
Backplane	HDD-BP	passive	Elec.	HDD Backplane	0	0	0	0,00	0,00	0,00	0,00	0,00	0,00
Power Consumption (ACOP-PS dissipation not considered)													
Power consumption when 2 HDDs are ON and 2 HDDs are in standby					5405	2785	2260	17,84	13,93	27,12	24,18	58,88	
Power consumption when 4 HDDs are ON plus CPU maximum consumption					5800	3785	3680	19,14	18,93	44,16			82,23
ACOP-PS Power Dissipation													
Power	ACOP-PS	on	Elec.	when 2 HDDs ON; 2 HDDs stdby				9,60	5,69	8,10		23,39	
Power	ACOP-PS	on	Elec.	when 4 HDDs are ON plus CPU max				10,31	7,73	13,19			31,23
				Estimate efficiency				0,65	0,71	0,77			
Power Consumption for ACOP Operative Modes													
ACOP Power Off					0	0	0	0,00	0,00	0,00		0,00	
ACOP Cold Start					5405	1785	840	17,84	8,93	10,08		36,84	
ACOP Warm Start					5405	1785	840	17,84	8,93	10,08		36,84	
ACOP Active Idle					5405	1785	840	17,84	8,93	10,08		36,84	
ACOP Active Recording (2 HDDs ON; 2 HDDs stdby)					5405	2785	2260	27,44	19,61	35,22		82,27	
ACOP Active Playback (2 HDDs ON; 2 HDDs stdby)					5405	2785	2260	27,44	19,61	35,22		82,27	
ACOP Recording and Playback (4 HDDs ON plus CPU max)					5800	3785	3680	29,45	26,65	57,35			113,45

Table 5-30 ACOP Power Budget

6. EMC REQUIREMENTS ASSESMENT AND VERIFICATION APPROACH

This section provides the list of the EMC and bonding-grounding requirements applicable to ACOP and the identification of the verification type to be applied.

6.1.1 EMC APPLICABLE DOCUMENTS

The AD1 Sections 7.1, 7.3 and 7.4 contain all the requirements that ACOP shall to be compliant with. Sections 7.2, 7.4.1, and 7.4.2 are not to be considered applicable due to the fact ACOP will be transported inside the Shuttle in power off condition.

6.1.1.1 EMC VERIFICATION

Verification of the applicable requirements given in AD1 will be carried out by test and/or review of design and/or analysis as defined in AD13.

6.1.2 EMC REQUIREMENTS

6.1.2.1 CE 01 CONDUCTED EMISSION REQUIREMENT

The ACOP shall comply with the narrow band emission between 30 Hz and 15 KHz on the DC current leads as specified in the AD1 Section 7.3.1.3.1. The emission limit shall be established considering that the ACOP requires an input current of 5A (TBC) on the 28Vdc nominal inlet (140W @28Vdc).

6.1.2.1.1 CE 01 VERIFICATION

The verification of the CE 01 EMC requirement shall be carried out in accordance with the requirements defined in the AD1 Section 7.3.1.3.2

The test shall be carried out in the noisiest operating mode

6.1.2.2 CE 03 CONDUCTED EMISSIONS

6.1.2.2.1 CE 03 REQUIREMENTS

ACOP shall comply with the narrow band emission between 15 KHz and 50 MHz on the DC current leads as specified in the AD1 Section 7.3.1.3.3

The emission limit shall be established considering that the unit requires the input current already specified in previous paragraphs.

6.1.2.2.2 CE 03 VERIFICATION

The verification of the CE 03 EMC requirement shall be carried out in accordance with the requirements defined in the AD1 Section 7.3.1.3.4

The test shall be carried out in the noisiest operating mode

6.1.2.3 CE 07 CONDUCTED EMISSIONS

6.1.2.3.1 CE 07 REQUIREMENTS

ACOP shall comply with the direct current input power leads spikes (in the time domain) as indicated in the AD1 Section 7.3.1.3.5. The purpose of the test is to measure in the time domain the unit induced effect on the input DC power quality, caused by cycling the ACOP power and changing the operating modes.

6.1.2.3.2 CE 07 VERIFICATION

The verification of the CE 07 EMC requirement shall be carried out in accordance with the requirements defined in the AD1 Section 7.3.1.3.6

6.1.2.4 CS01 CONDUCTED SUSCEPTIBILITY

6.1.2.4.1 CS 01 REQUIREMENT (30 HZ – 50 KHZ)

The ACOP Payload shall not produce an unsafe condition or one that could result in damage to ISS equipment or payload hardware and shall operate within the specification without performance degradation when subjected to electromagnetic energy injected on the power leads as specified in AD1 Section 7.3.1.4.2

6.1.2.4.2 CS 01 VERIFICATION

The verification of the CS 01 requirement shall be carried out in accordance with the directions given at Section 3.2.2.1 of the SSP-30238

6.1.2.5 CS 02 CONDUCTED SUSCEPTIBILITY

6.1.2.5.1 CS 02 REQUIREMENT (50 KHZ – 50 MHZ)

The ACOP shall not produce an unsafe condition or one that could result in damage to ISS equipment or payload hardware and shall operate within the specification without performance degradation when subjected to electromagnetic energy injected on the power leads as specified in AD1 Section 7.3.1.4.4.

6.1.2.5.2 CS02 VERIFICATION

The verification of the CS 02 requirement will be carried out in accordance with the Section 3.2.2.2 of the SSP-30238.

6.1.2.6 CS 06 CONDUCTED SUSCEPTIBILITY

6.1.2.6.1 CS 06 REQUIREMENT

The ACOP shall not produce an unsafe condition or one that could result in damage to ISS equipment or payload hardware and shall operate within the specification without performance degradation when subjected to electromagnetic energy injected on the power leads as specified in AD1 Section 7.3.1.4.6.

6.1.2.6.2 CS 06 VERIFICATION

The verification of the CS 06 requirement will be carried out by test in accordance with the Section 3.2.2.3 of the SSP-30238.

6.1.2.7 RE 02 RADIATED EMISSIONS

Electric field, 14 KHz – 10 GHz (narrow band), 13,5 – 15,5 GHz

6.1.2.7.1 RE 02 REQUIREMENT

ACOP shall not radiate in excess of the values specified in AD1 Section 7.3.1.5.4.

6.1.2.7.2 RE 02 VERIFICATION

The verification of the compliance with the RE 02 requirement shall be carried out by test, in accordance with the Section 3.2.3.1 of the SSP-30238.

6.1.2.8 RS 02 RADIATED SUSCEPTIBILITY

Magnetic induction field

6.1.2.8.1 RS 02 REQUIREMENT

The ACOP shall not produce an unsafe condition or one that could result in damage to ISS equipment or payload hardware when subjected sequentially when subjected to the test spikes specified in AD1 Section 7.3.1.6.3.

6.1.2.8.2 RS 02 VERIFICATION

The verification of the compliance with the RS02 requirement will be carried out by test. The test will be executed in accordance with the instructions given in Section 3.2.4.1 of the SSP-30238

6.1.2.9 RS 03 RADIATED SUSCEPTIBILITY

Electric field, 14 KHz to 20 GHz

6.1.2.9.1 RS 03 REQUIREMENTS

The ACOP shall not produce an unsafe condition or one that could result in damage to ISS equipment or payload hardware when subjected to the radiated electric field less than or equal to the values specified in AD1 Section 7.3.1.7.2.

6.1.2.9.2 RS 03 VERIFICATION

The RS03 requirement will be verified by test in accordance with the instructions given at Section 3.2.4.2 of the SSP-30238.

Since the unit is digital equipment the requirement of Section 3.2.4.2.3.9.3 is considered applicable for the modulation.

6.1.3 ADDITIONAL REQUIREMENTS

6.1.3.1 CORONA EFFECTS

6.1.3.1.1 CORONA REQUIREMENT

The ACOP shall be designed to preclude damaging by the corona effect in any ISS operating condition

6.1.3.1.2 CORONA VERIFICATION

It is understood that the compliance with the requirement defined in AD1 Section 7.3.2.3 is verified by the absence of corona effects during functional test.

6.1.3.2 STATIC ELECTRICITY

6.1.3.2.1 ELECTROSTATIC DISCHARGE REQUIREMENT

The un-powered ACOP shall not be damaged by electrostatic discharge (ESD) equal to or less than 4KV applied to the case or to any pin on external connectors.

If the ACOP may be damaged by ESD between 4 KV and 15 KV, they must have a label placed on the case in a location clearly visible in the installed position.

Handling and labeling of the units susceptible to ESD up to 15 KV shall be in accordance with MIL-STD-1686A

6.1.3.2.2 ESD VERIFICATION

The verification will be carried out by analysis or test. The ESD will be simulated by charging a 100pF capacitor and discharging it through a 1500 Ω resistor

6.1.3.3 LIGHTNING

6.1.3.3.1 LIGHTNING REQUIREMENT

ACOP shall be designed so that a failure due to a lightning strike will not propagate to the MPLM or the ISS

6.1.3.3.2 LIGHTNING VERIFICATION

The verification that the payload is designed to meet the lightning produced magnetic fields environment of the payload bay as specified in the IDD will be performed by analysis based on RS02 test results as suggested by AD13.

6.1.3.4 MAGNETIC FIELDS

6.1.3.4.1 MAGNETIC FIELDS FOR EXPRESS RACK PAYLOADS IN THE ISS REQUIREMENTS

ACOP shall not generate AC or DC magnetic fields greater than the limits defined in AD1 Sections 7.4.3.1 and 7.4.3.2.

6.1.3.4.2 MAGNETIC FIELDS FOR EXPRESS RACK PAYLOADS IN THE ISS VERFICATION

The requirements will be verified by test.

6.1.4 GROUNDING & BONDING

6.1.4.1 GROUNDING & BONDING REQUIREMENTS

ACOP shall meet the grounding and bonding requirements given in AD1 Sections 7.5 – 7.7 and in particular:

- ACOP shall be inserted and fixed into a Locker location of an EXPRESS Rack before being powered on
- ACOP will use the single point ground approach for the internally DC/DC generated secondary power lines (3.3V, 5V and 12V).
- the EXPRESS Rack 28Vdc primary power line will be maintained isolated from the ACOP chassis/structure by a minimum of 1 Mohm in parallel with a capacitance less than 10uF.
- the Express Rack 28Vdc primary power line will be kept isolated from ACOP secondary power voltages by a minimum of 1 Mohm

6.1.4.2 GROUNDING & BONDING VERIFICATION

Verification of the applicable requirements given in AD1 will be carried out by test and/or review of design and/or analysis as defined in AD13.

7. EMC ANALYSIS

7.1 GROUNDING / BONDING / ISOLATION

The ACOP electronics is housed in an aluminum box. The parts of the box are electrically connected together in order to offer a low impedance path, therefore the mechanical box will operate as a shield against the internally generated emissions and the externally generated emissions.

The ACOP shall be bonded via the bond path present in the EXPRESS Rack-to-payload power connector (pin D).

The bonding path to the Express Rack will allow:

- to conduct electrical faults current without creating thermal or electrical hazard
- to minimize differences in potential between all equipment.

The ACOP internal power lines are derived from the 28Vdc input line. The 28Vdc input line will be kept isolated from ground/structure by at least 1 Mohm (this applies to the alive and return line), in parallel with a capacitance of less than 10uF, according to AD1 Section 7.6 (Power Circuit Isolation and Grounding). The 28Vdc input line will be also isolated from the ACOP internal DC/DC generated power supplies by at least 1Mohm.

The Ethernet connection with the EXPRESS Rack RIC will be as per AD1 Section 7.7 (Signal Isolation and Grounding Requirements) for isolation and grounding.

The HRDL interfaces will use optic fiber cables as physical layer, therefore there will not be electrical connections.

One RS 422 Interface will be present only for ground test.

USB 2.0 ports will be present to be used by crew in nominal scenarios to connect portable devices (USB storage keys) to apply software updates.

7.2 DC-DC CONVERTER EMI FILTER

The MDI DC/DC Converters incorporate an integral input EMI filter that reduces the conducted emissions below the level of CE03 of MIL-STD-461C. The EMI filter also attenuates the effects of input CS06 spikes and CS01/CS02 conducted susceptibility. The filter consists of elements that block the conducted emissions from the power leads. In addition, the filter has elements that provide low impedance shunt paths for unwanted current.

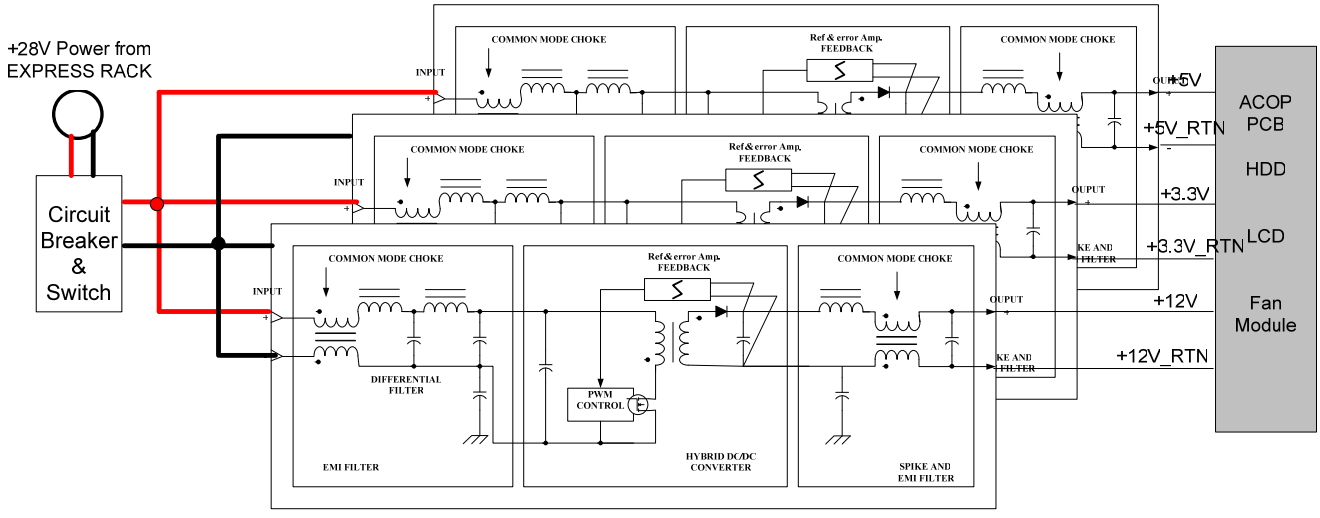

Figure 7-1 DC-DC Converter EMI Filter

The general filter schematic is shown in Figure 7-1. With the output common mode filter, uncontrolled conducted emissions will not allow to exit from the output leads of the converter.

On the power input side of each DC/DC converter the common mode currents are interrupted by a high inductance common mode choke. A shunt capacitor connected to the hybrid integrated circuit case allows the common mode input currents to be localized, instead of flowing out to the input leads.

Two stages of LC differential filtering are used to reduce ripple current levels. By using two cascaded higher frequency stages, each stage is physically smaller than a larger, lower frequency single stage.

On the output side of each DC/DC converter a common mode choke and a shunt capacitor to the hybrid integrated circuit case completely tame the common mode spikes. A small differential filter adds the final bit of filtering to the output leads. At above approximately 10 MHz, the output filters within the hybrid can become capacitive: external ferrite leads and small capacitors may be used to tame the residual high frequency spikes.

7.3 INRUSH CURRENT

There are no constraints on how fast or how slow the input voltage can be applied to the DC/DC converters. The typical input current as a function of time is shown below:

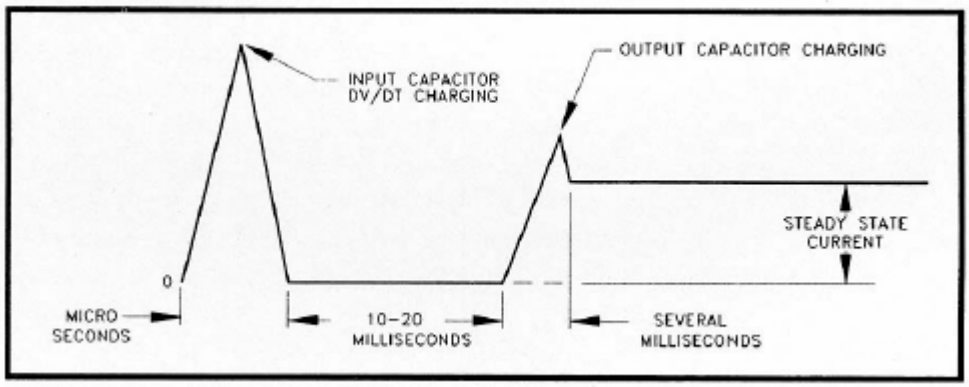

Figure 7-2 Typical input current waveform at DC/DC converters switch-on

There are two peaks in the current waveform. The first peak is due to input EMI filter capacitor charging. The capacitor charging peak current is dependent on the rate of rise of input voltage. Although the inductance and resistance of the input EMI filter limit the initial inrush current, the small cores in the filter tend to saturate during initial turn-on. The second peak is due to the converter coming on and supplying the load as well as the internal and external load capacitance. The initial inrush current due to capacitor charging will be highly dependent on the rate of rise of input voltage.

The input capacitance of the MDI DC/DC converters used in ACOP is:

- 13.5uF for the 5680 series (28V to 5V converter)
- 18.0uF for the 5193 series (28V to 3.3V converter)
- 24.0uF for the 5031 series (28V to 12V converter)

Therefore the total input capacitance of the three converters in parallel is 55.5uF. Considering that the input voltage is 28V, the inrush current is estimated to be within an acceptable level. The reverse energy requirement is estimated to be fulfilled as well.

7.4 CONDUCTED AND RADIATED EMISSION SOURCES

The main sources of conducted/radiated emissions are:

- ACOP DC/DC converters to generate the ACOP internal voltages
- CompactPCI bus traffic running at 33 MHz on the 5 slots ACOP-BP
- ACOP Single Board Computer
- Hard Disk Drives (mainly the disk motor control sections)
- Fans (mainly the motors)

In particular, the following clock frequencies are present in ACOP:

- 400 MHz and 33 MHz on the ACOP-SBC board (400 MHz for the Power PC chip and 33 MHz for the CompactPCI interface)
- 25 MHz for the VGA control logic on the ACOP-T101 board
- 48 MHz for the USB Controller on the ACOP-T101 board
- 50 MHz for the HRDL board ACOP-T102
- 66 MHz for the SATA interface on the ACOP-T103 board
- 50 MHz (TBC) for the Ethernet Interface on the ACOP-T103 board
- 100-110 KHz (TBC) for the DC/DC converters control logic.

8. GROUNDING PHILOSOPHY

The ACOP avionics, with respect to the overall grounding system, is based on the following concepts:

- The primary electrical power is isolated from ACOP chassis / locker by a minimum of 1 Mohm in parallel with a capacitance less than 10uF.
- Implementation of a galvanic isolation between the primary power bus and all the secondary internal or distributed powers (greater than 1 Mohm)
- All the secondary power references are connected together and to the ACOP structure in a single point represented by an internal bonding terminal.
- The metallic shells of all the ACOP external electrical connectors are electrically bonded to the ACOP bulkhead mount connector or the ACOP front panel case, with a DC resistance of less than 2.5 milliohms per joint.

The primary payload bond path for ACOP shall be through the EXPRESS Rack-to-payload power connector interface.

An internal to the ACOP Front Panel bonding strap will connect the movable part of the ACOP Front Panel (ACOP Door) to the fixed part (the bonding between the two parts of the ACOP Front Panel will not rely only on the friction hinges).

In Figure 8-1 the ACOP grounding philosophy is shown.

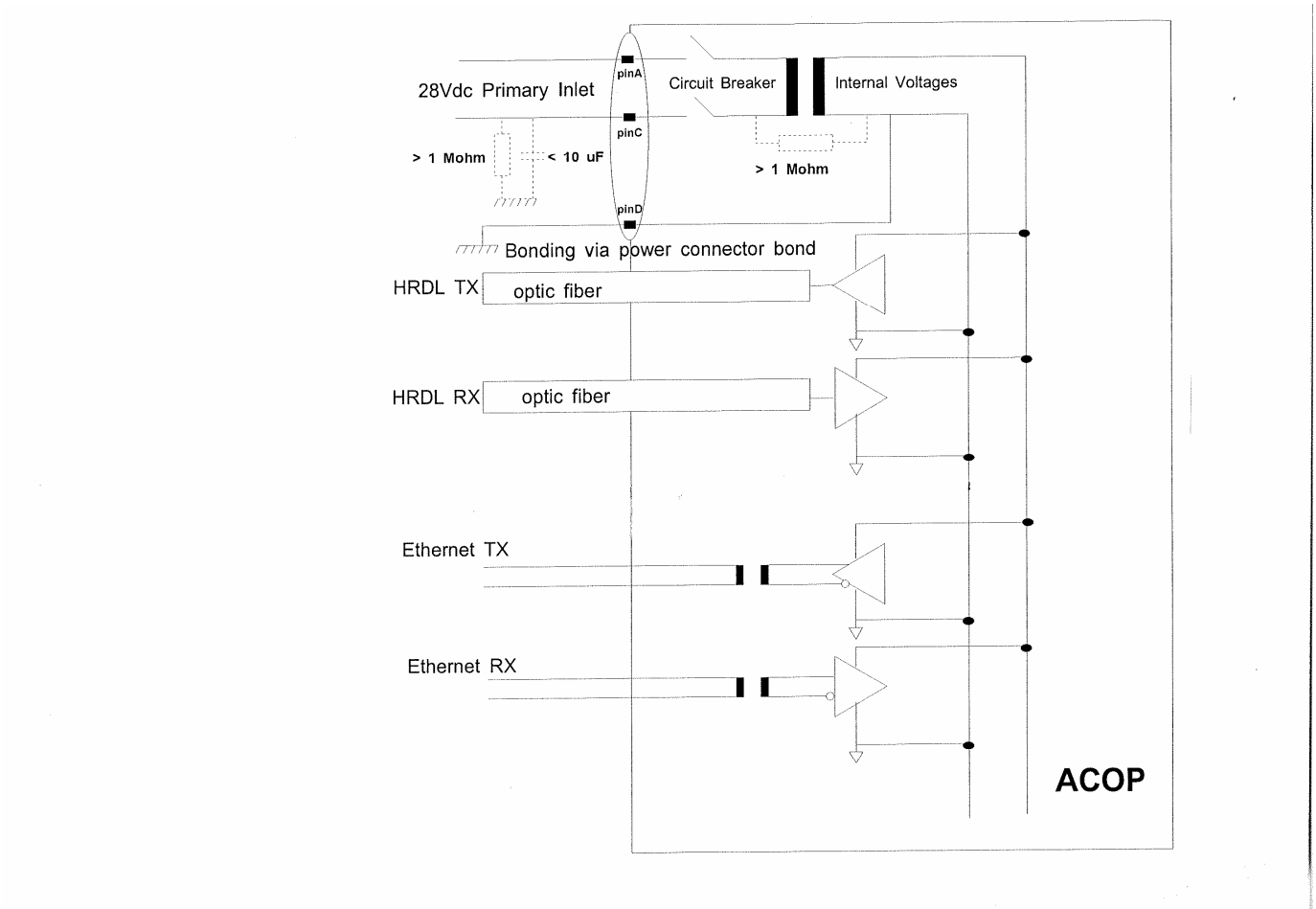

Figure 8-1 ACOP Grounding Philosophy